STANDARD
MICROSYSTEMS
CORPORATION

FDC37N972
ADVANCE INFORMATION

Advanced Notebook I/O Controller with Enhanced Keyboard Control and System Management

FEATURES

- 3.3V Operation With 5V Tolerant Buffers
- ACPI 1.0 and PC99 Compliant
- Three Power Planes
- ACPI Embedded Controller Interface
- Low Standby Current in Sleep Mode
- Configuration Register Set Compatible With ISA Plug-and-Play Standard (Version 1.0a)
- Serial IRQ Interface Compatible With Serialized IRQ Support for PCI Systems
- Floppy Disk Interface on Parallel Port
- 8051 Controller uses Parallel Port to Reprogram the Flash ROM
- Advanced Infrared Communications Controller (IrCC 2.0)
  - IrDA V1.1 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - Two IR Ports
  - Relocatable Base I/O Address
- 512k Byte Flash ROM Interface
  - 8051/Host CPU Multiplexed Interface
  - Sixteen 32K Pages - 8051 Keyboard BIOS
  - Eight 64K Pages - Host System BIOS
  - Embedded Controller uses Parallel Port to Reprogram Flash ROM
- ISA Host Interface With Clock Run Support and ACPI SCI Interface
  - 16 Bit Address Qualification
  - 8 Bit Data Bus
  - Zero Wait-State I/O Register Access
  - Shadowed Write Only registers
  - IOCHRDY for ECP, IRCC 2.0 and Flash Cycles
  - 15 Direct IRQs Including nSMI
  - Four 8 Bit DMA Channels
  - XNOR Test Chain
- High-Performance Embedded 8051 Keyboard and System Controller
  - Provides System Power Management
  - System Watch Dog Timer (WDT)
  - 8042 Style Host Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 2K Internal ROM, nEA Pin Select
  - 32K Bank Switchable External Flash ROM Interface
  - 256 Bytes Data RAM
  - On-Chip Control Registers Available via MOVX External Data Access Commands
  - Access to RTC and CMOS Registers
  - Up to 16x8 Keyboard Scan Matrix
  - Three 16 Bit Timer/Counters
  - Integrated TX/RX Serial Interface
  - Eleven 8051 Interrupt Sources
  - Thirty-Two 8 Bit, Host/8051 Mailbox Registers
  - Thirty Maskable Hardware Wake-Up Events Supported
  - Fast GATEA20
  - Fast CPU_RESET
  - Multiple Clock Sources and Frequencies
  - IDLE and SLEEP Modes
  - Fail-Safe Ring Oscillator
- Real Time Clock
  - MC146818 and DS1287 Compatible
  - 256 Bytes of Battery Backed CMOS in Two 128-Byte Banks
  - 128 Bytes of CMOS RAM Lockable in 4x32 Byte Blocks
  - 12 and 24 Hour Time Format
  - Binary and BCD Format

- <2μA Standby Current (typ)
- Two 8584-Style ACCESS.bus Controllers
- Four independent Hardware Driven PS/2 Ports
- General Purpose I/O
  - 22 I/O Pins
  - 12 Out Pins
  - Eight In Pins
- Two Programmable Pulse-Width Modulator Outputs
  - Independent Clock Rates
  - 6 Bit Duty Cycle Granularity
  - VCC1 and VCC2 operation mode
- Intelligent Auto Power Management
- 2.88MB Super I/O Floppy Disk Controller
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
  - Four DMA Options
  - Open-Drain/Push-Pull Configurable Output Drivers
  - Licensed CMOS 765B Floppy Disk Controller
  - Advanced Digital Data Separator
  - Software and Register Compatible With SMSC's Proprietary 82077AA Compatible Core
  - Low Power CMOS Design with Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - Supports Two Floppy Drives on the FDD Interface and Two Floppy Drives on the Parallel Port Interface
  - 12 mA FDD Interface Cable Drivers With Schmitt Trigger Inputs
- Licensed CMOS 765B Floppy Disk Controller Core
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - 12 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
- Enhanced Digital Data Separator
  - Low Cost Implementation
  - No Filter Components Required
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bi-directional Parallel Port
  - Enhanced Parallel Port EPP 1.7 and EPP 1.9 Compatible (IEEE 1284 Compliant) IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry to Prevent Printer Power-On Damage
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
  - 4 DMA Options
  - Microsoft and HP compatible High Speed Mode
  - 12 mA Output Drivers
- Serial Port
  - High-Speed NS16550A-Compatible UART with 16-Byte Send/Receive FIFOs
  - Programmable Baud Rate Generator Modem Control Circuitry Including 230k and 460k Baud
  - Relocatable to 480 Different Base I/O Addresses
  - 15 IRQ Options
- 208 Pin TQFP Package Options
- 208 Pin FBGA Package Options

GENERAL DESCRIPTION

The FDC37N972 is a 208-pin 3.3V ISA Host ACPI 1.0 and PC98 (/PC99)-compliant Ultra I/O Controller with Fast Infrared for mobile applications.

The FDC37N972 incorporates a high-performance 8051-based keyboard controller; a 512k byte Flash ROM interface; four PS/2 ports; a real-time clock; SMSC's true CMOS 765B floppy disk controller with advanced digital data separator and 16-byte data FIFO; an NS16C550A-compatible UART, SMSC's advanced Infrared Communications Controller (IrCC 2.0) with a UART and a Synchronous Communications Engine to provide IrDA v1.1 (Fast IR) capabilities; one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support; two 8584-style Access Bus controllers; a Serial IRQ peripheral agent interface; an ACPI Embedded Controller Interface; General Purpose I/O pins; two independently programmable pulse width modulators; two-floppy direct drive support; and maskable hardware wake-up events.

The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology, allowing for ease of testing and use.

The parallel port is compatible with IBM PC/AT architecture, as well as EPP and ECP. The 8051 controller can also take control of the parallel port interface to provide remote diagnostics or “Flashing” of the Flash memory.

The FDC37N972 has three separate power planes to provide “instant on” and system power management functions. Additionally, the FDC37N972 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. Wake-up events and ACPI-related functions are supported through the SCI Interface.

The FDC37N972’s configuration register set is compatible with the ISA Plug-and-Play Standard (Version 1.0a) and provides the functionality to support Windows '95. Through internal configuration registers, each of the FDC37N972's logical device's I/O address, DMA channel and IRQ channel may be programmed. There are 480 I/O address location options, 15 IRQ options, and four DMA channel options for each logical device.

The FDC37N972 does not require any external filter components and is, therefore, easy to use and offers lower system cost and reduced board area. The FDC37N972 is software and register compatible with SMSC's proprietary 82077AA core.

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PIN CONFIGURATION

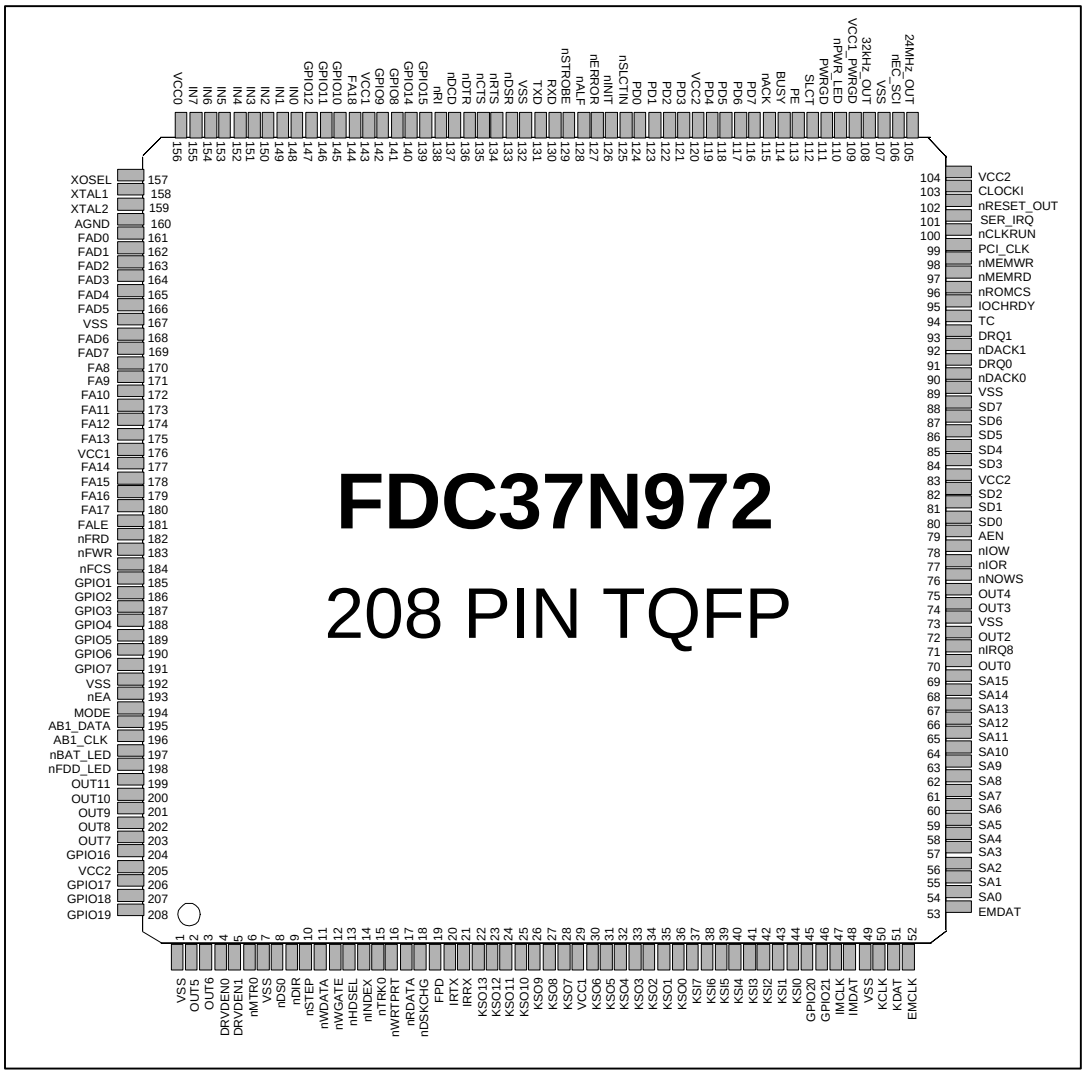


FIGURE 1 - FDC37N972 PIN CONFIGURATION
For FBGA BALL PAD Configuration refer to FIGURE 81 on Page 372.

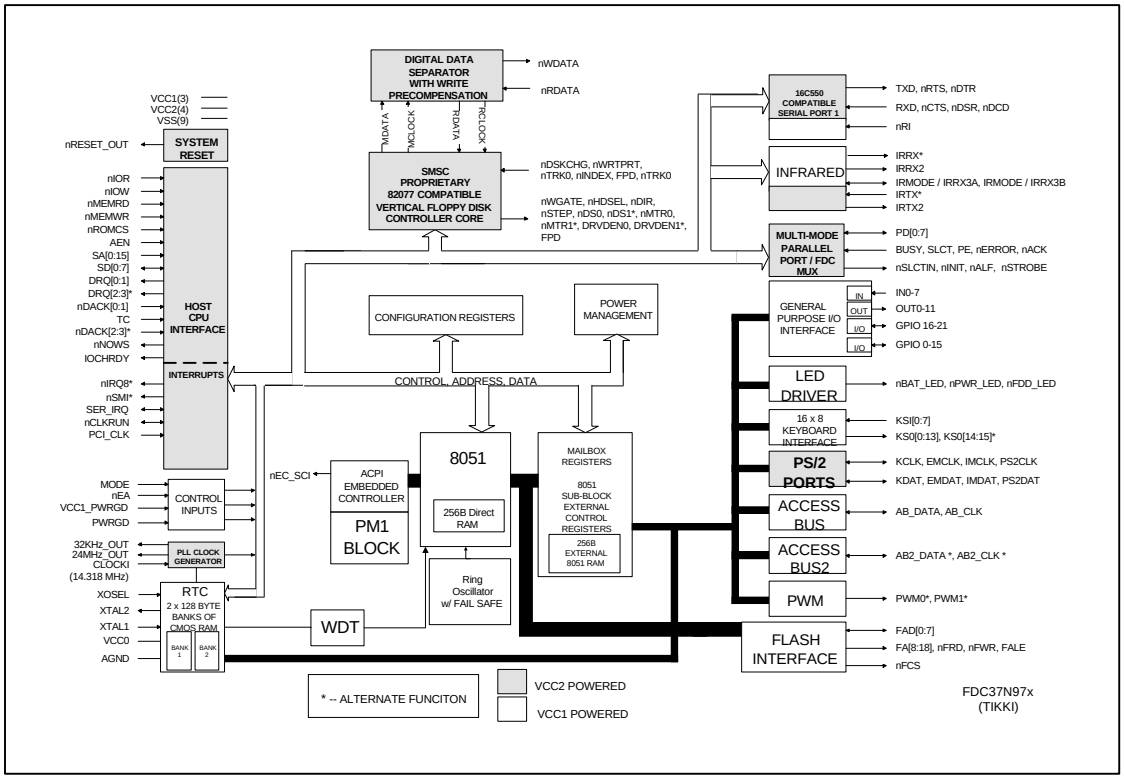


FIGURE 2 - FDC37N972 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

TABLE 1 - FDC37N972 PIN CONFIGURATION

TQFP PIN#	FGBA PIN#	NAME	TQFP PIN#	FGBA PIN#	NAME	TQFP PIN#	FGBA PIN#	NAME
1	A1	**VSS**	**39**	M3	KSI5	**77**	U8	nIOR
2	C2	OUT5	**40**	N4	KSI4	**78**	T9	nIOW
3	D4	OUT6	**41**	M1	KSI3	**79**	R9	AEN
4	B1	DRVDEN0	**42**	N2	KSI2	**80**	P10	SD0
5	C1	DRVDEN1	**43**	N3	KSI1	**81**	U9	SD1
6	D2	nMTR0	**44**	N1	KSI0	**82**	T10	SD2
7	D3	**VSS**	**45**	P1	GPIO20	**83**	R10	**VCC2**
8	E4	nDS0	**46**	P2	GPIO21	**84**	P11	SD3
9	D1	nDIR	**47**	P3	IMCLK	**85**	U10	SD4
10	E2	nSTEP	**48**	R1	IMDAT	**86**	T11	SD5
11	E3	nWDATA	**49**	T1	**VSS**	**87**	R11	SD6
12	F4	nWGATE	**50**	R2	KCLK	**88**	P12	SD7
13	E1	nHDSEL	**51**	R3	KDAT	**89**	U11	**VSS**
14	F2	nINDEX	**52**	T2	EMCLK	**90**	T12	nDACK0
15	F3	nTRK0	**53**	U1	EMDAT	**91**	R12	DRQ0
16	G4	nWRTPRT	**54**	T3	SA0	**92**	P13	nDACK1
17	F1	nRDATA	**55**	P4	SA1	**93**	U12	DRQ1
18	G2	nDSKCHG	**56**	U2	SA2	**94**	T13	TC
19	G3	FPD	**57**	U3	SA3	**95**	R13	IOCHRDY
20	H4	IRTX	**58**	T4	SA4	**96**	U13	nROMCS
21	G1	IRRX	**59**	R4	SA5	**97**	U14	nMEMRD
22	H2	KSO13	**60**	P5	SA6	**98**	T14	nMEMWR
23	H3	KSO12	**61**	U4	SA7	**99**	R14	PCI_CLK
24	J4	KSO11	**62**	T5	SA8	**100**	U15	nCLKRUN
25	H1	KSO10	**63**	R5	SA9	**101**	U16	SER_IRQ
26	J2	KSO9	**64**	P6	SA10	**102**	T15	nRESET_OUT
27	J3	KSO8	**65**	U5	SA11	**103**	R15	CLOCKI
28	K4	KSO7	**66**	T6	SA12	**104**	T16	**VCC2**
29	J1	**VCC1**	**67**	R6	SA13	**105**	U17	24MHz_OUT
30	K2	KSO6	**68**	P7	SA14	**106**	R16	nEC_SCI
31	K3	KSO5	**69**	U6	SA15	**107**	P14	**VSS**
32	L4	KSO4	**70**	T7	OUT0	**108**	T17	32kHz_OUT
33	K1	KSO3	**71**	R7	OUT1	**109**	R17	VCC1_ PWRGD
34	L2	KSO2	**72**	P8	OUT2	**110**	P16	nPWR_LED
35	L3	KSO1	**73**	U7	**VSS**	**111**	P15	PWRGD
36	M4	KSO0	**74**	T8	OUT3	**112**	N14	SLCT
37	L1	KSI7	**75**	R8	OUT4	**113**	P17	PE
38	M2	KSI6	**76**	P9	nNOWS	**114**	N16	BUSY

TQFP PIN#	FGBA PIN#	NAME	TQFP PIN#	FGBA PIN#	NAME	TQFP PIN#	FGBA PIN#	NAME
115	N15	nACK	**147**	E15	GPIO12	**179**	C10	FA16
116	M14	PD7	**148**	E17	IN0	**180**	D9	FA17
117	N17	PD6	**149**	D17	IN1	**181**	A10	FALE
118	M16	PD5	**150**	D16	IN2	**182**	B9	nFRD
119	M15	PD4	**151**	D15	IN3	**183**	C9	nFWR
120	L14	**VCC2**	**152**	C17	IN4	**184**	D8	nFCS
121	M17	PD3	**153**	B17	IN5	**185**	A9	GPIO1
122	L16	PD2	**154**	C16	IN6	**186**	B8	GPIO2
123	L15	PD1	**155**	C15	IN7	**187**	C8	GPIO3
124	K14	PD0	**156**	B16	**VCC0**	**188**	D7	GPIO4
125	L17	NSLCTIN	**157**	A17	XOSEL	**189**	A8	GPIO5
126	K16	nINIT	**158**	B15	XTAL1	**190**	B7	GPIO6
127	K15	nERROR	**159**	D14	XTAL2	**191**	C7	GPIO7
128	J14	nALF	**160**	A16	**AGND**	**192**	D6	**VSS**
129	K17	nSTROBE	**161**	A15	FAD0	**193**	A7	nEA
130	J16	RXD	**162**	B14	FAD1	**194**	B6	MODE
131	J15	TXD	**163**	C14	FAD2	**195**	C6	AB1_DATA
132	H14	**VSS**	**164**	D13	FAD3	**196**	D5	AB1_CLK
133	J17	nDSR	**165**	A14	FAD4	**197**	A6	nBAT_LED
134	H16	nRTS	**166**	B13	FAD5	**198**	B5	nFDD_LED
135	H15	nCTS	**167**	C13	**VSS**	**199**	C5	OUT11
136	G14	nDTR	**168**	D12	FAD6	**200**	A5	OUT10
137	H17	nDCD	**169**	A13	FAD7	**201**	A4	OUT9
138	G16	nRI	**170**	B12	FA8	**202**	B4	OUT8
139	G15	GPIO15	**171**	C12	FA9	**203**	C4	OUT7
140	F14	GPIO14	**172**	D11	FA10	**204**	A3	GPIO16
141	G17	GPIO8	**173**	A12	FA11	**205**	A2	**VCC2**
142	F16	GPIO9	**174**	B11	FA12	**206**	B3	GPIO17
143	F15	**VCC1**	**175**	C11	FA13	**207**	C3	GPIO18
144	E14	FA18	**176**	D10	**VCC1**	**208**	B2	GPIO19
145	F17	GPIO10	**177**	A11	FA14			
146	E16	GPIO11	**178**	B10	FA15			

VCC2 VCC1 VCC0

Device functions per pin are shown in TABLE 2. Buffer Modes symbols in TABLE 2 are described in Table 3. Multifunction pins are summarized in Table 4, including a multiplex controls reference.

The pins and descriptions in Table 2 are organized by primary pin function. For example, the PS2 Serial Clock and PS2 Serial Data pins are technically part of the KEYBOARD AND MOUSE INTERFACE but are listed in the GENERAL PURPOSE I/O INTERFACE because the GPIO function of these pins is the default.

TABLE 2 - PIN FUNCTION DESCRIPTION

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
FDD INTERFACE (15) The following FDC output pins can be configured as either Open Drain outputs capable of sinking 12mA (OD12) or as push-pull outputs capable of driving 6mA and sinking 12mA (O12). The FDC output pins must tristate when the FDC is in powerdown mode (The board designer must provide external pull-up resistors on these output pins).					
4		DRVDEN0	Drive Density Select 0	VCC2	(O12/OD12)
5		DRVDEN1	Drive Density Select 1	VCC2	(O12/OD12)
6		nMTR0	Motor On 0	VCC2	(O12/OD12)
8		nDS0	Drive Select 0	VCC2	(O12/OD12)
9		nDIR	Step Direction	VCC2	(O12/OD12)
10		nSTEP	Step Pulse	VCC2	(O12/OD12)
11		nWDATA	Write Disk Data	VCC2	(O12/OD12)
12		nWGATE	Write Gate	VCC2	(O12/OD12)
13		nHDSEL	Head Select	VCC2	(O12/OD12)
14		nINDEX	Index Pulse Input	VCC2	IS
15		nTRK0	Track 0	VCC2	IS
16		nWRTPRT	Write Protected	VCC2	IS
17		nRDATA	Read Disk Data	VCC2	IS
18		nDSKCHG	Disk Change	VCC2	IS
19		FPD	Floppy Power Down Output Control	VCC2	O8
PCI POWER MANAGEMENT AND SIRQ INTERFACE (4)					
106	7	nEC_SCI	Power Management Event	VCC1	PCI_OD
99		PCI_CLK	PCI Clock	VCC2	PCI_ICLK
101		SER_IRQ	Serial IRQ	VCC2	PCI_IO
100		nCLKRUN	PCI Clock Control	VCC2	PCI_OD
ISA HOST INTERFACE (37)					
80: 82, 84: 88		SD[7:0]	System Data Bus	VCC2	IO12
54: 69		SA[15:0]	System Address Bus	VCC2	I
96		nROMCS	ROM Chip Select	VCC2	I
79		AEN	Address Enable	VCC2	I
95		IOCHRDY	I/O Channel Ready	VCC2	OD12
91, 93		DRQ[1:0]	DMA Requests	VCC2	O12

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
90, 92		NDACK[1:0]	DMA Acknowledge	VCC2	I
94		TC	Terminal Count	VCC2	I
77		nIOR	I/O Read	VCC2	I
78		nIOW	I/O Write	VCC2	I
97		nMEMRD	Memory Read	VCC2	I
98		nMEMWR	Memory Write	VCC2	I
76		nNOWS	No Wait State	VCC2	OD12
FLASH ROM INTERFACE (23)					
161: 166, 168, 169		FAD[7:0]	Flash Address/Data[7:0] Bus	VCC1	IO8
170: 175, 177: 180		FA[8:17]	Flash Address[17:8] **NOTE**: Upper Address bit FA18 is multiplexed on GPIO13	VCC1	O8
144	5	FA18/ GPIO13 (WK_SE17)	Flash Address 18 General Purpose I/O	VCC1	O8/IO8
182		nFRD	Flash Memory Read	VCC1	O8
183		nFWR	Flash Memory Write	VCC1	O8
181		FALE	Flash Address Latch Enable	VCC1	O8
184	5	nFCS/ GPIO0 (WK_SE02)	Flash ROM Chip Select General Purpose I/O	VCC1	O8/IO8
KEYBOARD AND MOUSE INTERFACE (29)					
30: 36, 24: 28		KSO[0:11]	Keyboard Scan Outputs (14×8). NOTE: GPIO4 and GPIO5 can be configured as KSO14 and KSO15 (16×8).	VCC1	OD4
23	3	KSO12/ OUT8/ KBRST	Keyboard Scan Output General Purpose Output CPU_RESET	VCC1	OD4/OD4/ OD4
22	11	KSO13/ GPIO18	Keyboard Scan Output General Purpose I/O	VCC1	OD4/IOD4
37:44		KSI[0:7]	Keyboard Scan Inputs	VCC1	ISP
193		nEA	External Access for 2k ROM	VCC1	I
52		EMCLK	EM Serial Clock	VCC2	IOD16
53		EMDAT	EM Serial Data	VCC2	IOD16
47		IMCLK	IM Serial Clock	VCC2	IOD16
48		IMDAT	IM Serial Data	VCC2	IOD16
51		KDAT	Keyboard Data	VCC2	IOD16

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
50		KCLK	Keyboard Clock	VCC2	IOD16
GENERAL PURPOSE I/O INTERFACE (40)					
70	7,8	OUT0 (SCI)	General Purpose Output (SCI)	VCC1	(O12/OD12)
71	3	OUT1/ nIRQ8	General Purpose Output/ Active Low RTC IRQ	VCC1	O12/O12
72		OUT2	General Purpose Output	VCC1	O12
74		OUT3/ FRW	General Purpose Output Inverted Flash ROM Memory Write	VCC1	O12/O12
75		OUT4	General Purpose Output	VCC1	O12
2	3	OUT5/ nDS1/ KBRST	General Purpose Output FDD Drive Select 1[3] CPU_RESET[3]	VCC1	O12/(O12/ OD12)/O12
3	3	OUT6/ nMTR1	General Purpose Output FDD Motor On 1	VCC1	O12/(O12/ OD12)
203	3	OUT7/ nSMI	General Purpose Output SMI Output	VCC1	O12/OD12
202	3	OUT8/ DRQ2/ KBRST	General Purpose Output DMA Request CPU_RESET	VCC1	O12/O12/ O12
201	3	OUT9/ DRQ3	General Purpose Output DMA Request	VCC1	O12/O12
200		OUT10/ PWM0	General Purpose Output Pulse Width Modulator Output	VCC1	O12/O12
199		OUT11/ PWM1	General Purpose Output Pulse Width Modulator Output	VCC1	O12/O12
148	4	IN0 (WK_EE4)	General Purpose Input	VCC1	I
149	4	IN1 (WK_EE2)	General Purpose Input	VCC1	I
150	4	IN2 (WK_EE3)	General Purpose Input	VCC1	I
151		IN3 (nGPWKUP)	General Purpose Input (General Purpose Wake Up)	VCC1	I
152	5	IN4 (WK_SE00)	General Purpose Input	VCC1	I
153	5	IN5 (WK_SE01)	General Purpose Input	VCC1	I
154	5	IN6 (WK_SE05)	General Purpose Input	VCC1	I
155	4	IN7 (WK_EE1)	General Purpose Input	VCC1	I
185	5	GPIO1 (WK_SE03)	General Purpose I/O	VCC1	IO8

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
186	5	GPIO2 (WK_SE04)	General Purpose I/O	VCC1	IO8
187	6	GPIO3 (TRIGGER)	General Purpose I/O (Interrupt 1 Event)	VCC1	IO8
188	5	GPIO4 (WK_SE07)/ KSO14	General Purpose I/O Keyboard Scan Output	VCC1	IO8/OD8
189	5	GPIO5 (WK_SE10)/ KSO15	General Purpose I/O Keyboard Scan Output	VCC1	IO8/OD8
190	5	GPIO6 (WK_SE11)/ IRMODE/IRRX3A	General Purpose I/O FIR Mode Output or 2nd Receive Input	VCC1	IO8/(O8/I)
191	5, 8	GPIO7 (WK_SE06)[5]	General Purpose I/O	VCC1	(IO8/IOD8)[8]
141	5	GPIO8 (WK_SE12)/ IRRX2	General Purpose I/O IR Receive Input	VCC1	IO8/I
142	1, 5	GPIO9 (WK_SE13)/ IRTX2	General Purpose I/O IR Transmit Output	VCC1	IO12/O12
145	5	GPIO10 (WK_SE14)/ IRMODE/IRRX3B	General Purpose I/O FIR Mode Output or 2nd Receive Input	VCC1	IO8/O8/ (O8/I)
146	5	GPIO11 (WK_SE15)/ AB2_DATA	General Purpose I/O ACCESS.bus 2 Serial Data	VCC1	IO12/IOD12
147	5	GPIO12 (WK_SE16)/ AB2_CLK	General Purpose I/O ACCESS.bus 2 Clock	VCC1	IO12/IOD12
140	5	GPIO14 (WK_SE20)	General Purpose I/O	VCC1	IO8
139	5	GPIO15 (WK_SE21)	General Purpose I/O	VCC1	IO8
204	5	GPIO16 (WK_SE22)[5]	General Purpose I/O	VCC1	IO8
206	3, 5	GPIO17 (WK_SE23)/ GATEA20	General Purpose I/O KBD GATEA20 Output	VCC1	IO8/O8

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
207	5	GPIO18 (WK_SE27)/ nDACK2	General Purpose I/O/ DMA Acknowledge	VCC1	IO8/I
208	5	GPIO19 (WK_SE24)/ nDACK3	General Purpose I/O/ DMA Acknowledge	VCC1	IO8/I
45	3, 5	GPIO20 (WK_SE25)/ PS2CLK/ 8051RX/	General Purpose I/O PS2 Serial Clock 8051 RX Input	VCC1	IOD16/ IOD16/I
46	3,5	GPIO21 (WK_SE26)/ PS2DAT/ 8051TX	General Purpose I/O PS2 Serial Data 8051 TX Input	VCC1	IOD16/ IOD16/ OD16
INFRARED INTERFACE (2)					
21		IRRX	IR Receive Input	VCC1	I
20	1	IRTX	IR Transmit Output	VCC2	O12
PARALLEL PORT INTERFACE (17)					
126		nINIT/ nDIR	Initiate Output FDC Direction Control	VCC2	(OD14/ OP14)/OD14
125		nSLCTIN/ nSTEP	Printer Select Input FDC Step Pulse	VCC2	(OD14/ OP14)/OD14
124		PD0/ nINDEX	Port Data 0 FDC Index	VCC2	IOP14/I
123		PD1/ nTRK0	Port Data 1 FDC Track 0	VCC2	IOP14/I
122		PD2/ nWRTPRT	Port Data 2 FDC Write Protected	VCC2	IOP14/I
121		PD3/ nRDATA	Port Data 3 FDC Read Disk Data	VCC2	IOP14/I
119		PD4/ nDSKCHG	Port Data 4 FDC Disk Change	VCC2	IOP14/I
118		PD5	Port Data 5	VCC2	IOP14
117		PD6/ nMTR0	Port Data 6 FDC Motor On 0	VCC2	IOP14/OD14
116		PD7	Port Data 7	VCC2	IOP14
112		SLCT/ nWGATE	Printer Selected Status FDC Write Gate	VCC2	I/OD12
113		PE/ nWDATA	Paper End FDC Write Data	VCC2	I/OD12
114		BUSY/ nMTR1	Busy FDC Motor On 1	VCC2	I/OD12

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
115		nACK/ nDS1	Acknowledge FDC Drive Select 1	VCC2	I/OD12
127		nERROR/ nHDSEL	Error FDC Head Select	VCC2	I/OD12
128		nALF/ DRVDEN0	Autofeed Output FDC Density Select 0	VCC2	(OD14/OP14)/ OD14
129		nSTROBE/ nDS0	Strobe Output FDC Drive Select 0	VCC2	(OD14/OP14)/ OD14
SERIAL PORT INTERFACE (8)					
130		RXD	Receive Data	VCC2	I
131		TXD	Transmit Data	VCC2	O12
133		nDSR	Data Set Ready	VCC2	I
134		nRTS	Request to Send	VCC2	O8
135		nCTS	Clear to Send	VCC2	I
136		nDTR	Data Terminal Ready	VCC2	O8
138		nRI	Ring Indicator	VCC1	I
137		nDCD	Data Carrier Detect	VCC2	I
MISCELLANEOUS (11)					
108		32kHz_OUT	32.768kHz Output Clock --The 32 KHz output is enabled / disabled by setting / clearing bit-0 of the Output Enable 8051 memory mapped register. When disabled the 32 KHz_OUT pin is driven low. The 32 KHz_OUT pin defaults to the disabled state on VCC1 POR.	VCC1	O8
105		24MHz_OUT	24MHz Clock Output Programmable Clock Output. 1.8432 MHz (default = 24 MHz/13) 14.318 MHz 16 MHz 24 MHz 48 MHz	VCC2	O24
103		CLOCKI	14.318MHz Clock Input	VCC2	ICLK
194		MODE	Configuration Ports Base Address Select	VCC1	I
157	10	XOSEL	External 32kHz Clock Enable Input	VCC0	I

TQFP PIN#	NOTES	NAME	DESCRIPTION	POWER PLANE	BUFFER MODES[2]
109	9	VCC1_PWRGD	VCC1 Power Good Input. The trailing edge of VCC1 POR is released 20ms from the assertion of this pin. If this pin is pulled low while VCC1 is valid, then VCC1 POR will be asserted and held until 20ms from re-assertion of this pin. This pin has an internal weak (90µA) pull-up to VCC1.	VCC1	IP
102		nRESET_OUT	System Reset	VCC2	O8
197		nBAT_LED	Battery LED (0 = ON)	VCC1	OD12
110		nPWR_LED	Power LED (0 = ON)	VCC1	OD12
198		nFDD_LED	Floppy LED (0 = ON). This pin is asserted whenever either DRVSEL1 or DRVSEL0 is asserted or controlled by the 8051.	VCC1	OD12
111	9	PWRGD	VCC2 Power Good Input	VCC1	I
ACCESS BUS INTERFACE (2)					
195		AB1_DATA	ACCESS.bus 1 Serial Data	VCC1	IOD12
196		AB1_CLK	ACCESS.bus 1 Clock	VCC1	IOD12
REAL TIME CLOCK INTERFACE (2)					
158		XTAL1	32.768kHz Crystal Input	VCC0	ICLK2
159	10	XTAL2	32.768kHz Crystal Output	VCC0	(OCLK2/I)
POWER PLANES					
156		VCC0	RTC (V_{BAT}) Supply Voltage		
29, 143, 176,		VCC1	+3.3V ± 5% Main Battery Supply		
83, 104, 120, 205		VCC2	+3.3V ± 5% Switched AC/Main Battery Supply		
160		AGND	Analog Ground		
1,7,49, 73, 89, 107, 132, 167, 192		VSS	Digital Ground		

NOTE 1: These pins default to “output”, “low” to prevent infrared transceiver damage (see Section **IRTX Output Pins** *DEFAULT*).

NOTE 2: Buffer Modes per function on multiplexed pins are separated by a slash “/”; e.g., a pin with two multiplexed functions where the primary function is an input and the secondary function is an 8mA bidirectional driver is represented as “I/IO8”. Buffer Modes in parenthesis represent multiple buffer modes for a single pin function.

NOTE 3: This pin is tristated when PWRGD is inactive and the pin is configured as a VCC2-powered alternate function.

NOTE 4: These devices can generate wake-up events on either edge of the signal that is applied when the pin is configured as an input. The interrupts are masked by the Wake-up Mask Register bits.

NOTE 5: These devices can generate wake-up events on selectable edges of the signal that is applied when the pin is configured as an input. The interrupts are masked by the Wake-up Mask Registers and selected edges are programmed via the Edge Select registers (see section **8051 Internal PARALLEL** on page 170).

NOTE 6: This interrupt is masked by INT1 Mask Register bit 3. GPIO3 is the only GPIO pin which does not generate a wakeup event.

NOTE 7: The nEC_SCI pin can be controlled by hardware and 8051 software. The nEC_SCI pin can drive either the ACPI Run-time GPE Chipset input or the Wake GPE Chipset input (**FIGURE 7**). Depending how the nEC_SCI pin is used, other ACPI-related SCI functions may be best supplied by FDC37N972 general purpose output OUT0.

NOTE 8: OUT0 and GPIO7 are suitable as an SCI output pin because the buffer type can be configured as a push-pull or open-drain output (see a description of the MISC21 and MISC23 bits in **Multiplexing_3 Register** on page 278).

NOTE 9: Input levels for the PWRGD and VCC1_PWRGD pins are rail-to-rail ±400mV; e.g., PWRGD V_{IL} = .4V max, PWRGD V_{IH} = 2.7V min. @ VCC1 min.

NOTE 10: The function of these pins are described in Section **32kHz Clock Input** The FDC37N972 uses the XOSEL pin to select either a 32.768kHz input clock or a 32.768kHz crystal to drive the Real Time Clock Interface (Table 2 **- PIN FUNCTION DESCRIPTION).**

When XOSEL = ‘0’, the RTC uses a 32.768kHz crystal connected between the XTAL1 and XTAL2 pins. When XOSEL = ‘1’, the RTC is driven by a 32.768kHz single-ended clock source connected to THE **XTAL2 PIN.**

NOTE: ICC0 ≥ 10µA for time-keeping operations under VCC0 using a single-ended clock source. ICC1 = 30µA under VCC1 using a single-ended clock source.

NOTE 11: The GPIO18 alternate function of the KS013 pin has no wake-up capability (see note following).

TABLE 3 - BUFFER MODE LEGEND

BUFFER SYMBOL	DESCRIPTION
I	Input
IO12	Bidirectional – 12mA sink, 6mA source
IO8	Bidirectional – 8mA, 4mA source
IOD16	Input, open drain output – 16mA sink
IOD8	Input, open drain output – 8mA sink
IOP14	Bidirectional – 14mA sink, 14mA source, backdrive protected
IP	Input with pullup
IS	Schmitt trigger input
ISP	Schmitt trigger input with pullup
O12	Output – 12mA, 6mA source
O8	Output – 8mA, 4mA source
OD12	Open drain – 12mA sink
OD14	Open drain – 14mA sink
OD16	Open drain – 16mA sink
OD4	Open drain – 4mA sink
OD8	Open drain – 8mA sink
OP14	Output – 14mA sink, 14mA source, backdrive protected
PCI_ICLK	PCI clock input
PCI_IO	PCI bidirectional
PCI_OD	PCI open drain
ICLK	Clock input
ICLK2	Clock input 2
OCLK2	Clock output 2
O24	Output – 12mA, 6mA source

TABLE 4 - ALTERNATE FUNCTION PINS

DEFAULT FUNCTION[2]		ALTERNATE FUNCTION #1		ALTERNATE FUNCTION #2		MULTIPLEX CONTROLS
OUT1	VCC1	nIRQ8[3]	VCC2	-		MISC0
OUT3	VCC1	FWR	VCC1	-	-	ALT WRITE SELECT[6]
OUT5	VCC1	nDS1[3]	VCC2	KBRST[3]	VCC2	MISC[5, 22][5]
OUT6	VCC1	nMTR1[3]	VCC2	-	-	MISC5
OUT7	VCC1	nSMI[3]	VCC2	-		MISC18[1]
OUT8	VCC1	DRQ2[3]	VCC2	KBRST[3]	VCC2	MISC[17,10, 6]
OUT9	VCC1	DRQ3[3]	VCC2	-		MISC11
OUT10	VCC1	PWM0	VCC1	-		MISC4
OUT11	VCC1	PWM1	VCC1	-		MISC12[1]
nFCS	VCC1	GPIO0	VCC1	-		MISC19[1]
GPIO4	VCC1	KSO14	VCC1	-		MISC9
GPIO5	VCC1	KSO15	VCC1	-		
GPIO6	VCC1	IRMODE/IRRX3A[3]	VCC2	-		MISC[14:13]
GPIO8	VCC1	IRRX	VCC1	-		MISC[2,7]
GPIO9	VCC1	IRTX[4]	VCC2	-		
GPIO10	VCC1	IRMODE/IRRX3B[3]	VCC2	-		MISC[16:15]
GPIO11	VCC1	AB2_DATA	VCC1			MISC20
GPIO12	VCC1	AB2_CLK	VCC1			
FA18	VCC1	GPIO13	VCC1	-		MISC8[1]
GPIO17	VCC1	GATEA20[3]	VCC1	-		MISC6
GPIO18	VCC1	nDACK2	VCC1	-		MISC17
GPIO19	VCC1	nDACK3	VCC1	-		MISC11
GPIO20	VCC1	PS2CLK[3]	VCC2	8051RX	VCC1	MISC[3, 1]
GPIO21	VCC1	PS2DAT[3]	VCC2	8051TX	VCC1	
KSO12	VCC1	OUT8	VCC1	KBRST[3]	VCC2	MISC[17, 10, 6]
KSO13	VCC1	GPIO18	VCC1	-		MISC17

DEFAULT FUNCTION[2]		ALTERNATE FUNCTION #1		ALTERNATE FUNCTION #2		MULTIPLEX CONTROLS
nINIT	VCC2	nDIR	VCC2	-		CR25[4:3]
nSLCTIN	VCC2	nSTEP	VCC2	-		
PD0	VCC2	nINDEX	VCC2	-		
PD1	VCC2	nTRK0	VCC2	-		
PD2	VCC2	nWRTPRT	VCC2	-		
PD3	VCC2	nRDATA	VCC2	-		
PD4	VCC2	nDSKCHG	VCC2	-		
PD6	VCC2	nMTR0	VCC2	-		
SLCT	VCC2	nWGATE	VCC2	-		
PE	VCC2	nWDATA	VCC2	-		
BUSY	VCC2	nMTR1	VCC2	-		
nACK	VCC2	NDS1	VCC2	-		
nERROR	VCC2	NHDSEL	VCC2	-		
nALF	VCC2	DRVDEN0	VCC2	-		
nSTROBE	VCC2	NDS0	VCC2	-		

NOTE 1: See a description in Section **MULTIFUNCTION PIN** on page 271.

NOTE 2: The FDC37N972 pins are identified by primary pin function (see DESCRIPTION OF PIN FUNCTIONS on page 11). Note that some functions are available on more than one pin; e.g., OUT8, GPIO18 and KBRST.

NOTE 3: When this pin is configured as an alternate function output and PWRGD is inactive, i.e. VCC2 is 0v, the pin will tri-state to prevent back-biasing of external circuitry (see Section **General Purpose I/O (GPIO)** on page 265).

NOTE 4: This pin defaults to “output”, “low” for both the default (GPIO) function and the alternate (IRTX) function, regardless of the state of PWRGD (see Section **General Purpose I/O (GPIO)** on page 265).

NOTE 5: MISC5 must be inactive for MISC22 to enable KBRST.

NOTE 6: The ALT WRITE SELECT bit is in the Flash Configuration Register (see Section **ALT WRITE SELECT Bit,** D3 on page 197).

There are three power planes in the FDC37N972 V_{CC0}, V_{CC1}, and V_{CC2} with the following power sequencing requirement:

1. V_{CC2} shall have power applied simultaneously with or after V_{CC1}.
2. V_{CC1} shall have power applied simultaneously with or after V_{CC0}.

All internal components which utilize V_{CC0} power plane are switched internally between the VCC1 and VCC0 pins according to VCC1_PWRGD

See Table 5 for power consumption in various states.

Two FDC37N972 power supply configurations can be utilized. These power supply configuration types fundamentally differ upon the need for a backup battery (V_{BAT}) connection to V_{CC0}.

TYPE 1 devices do not require a V_{CC0} battery connection. Power supply requirements for TYPE 1 devices are as follows: V_{CC0} is tied to V_{SS}, V_{CC1} is connected to the main battery supply, and V_{CC2} is switched from either the main battery or AC power if available. In this configuration all internal components which utilize V_{CC0} power plane are switched internally to the VCC1 upon POR according to VCC1_PWRGD.

TYPE 2 devices require a V_{CC0} battery connection. Power supply requirements for TYPE 2 devices are as follows: V_{CC0} is connected to a backup battery (V_{BAT}), V_{CC1} is connected to the main battery supply, and V_{CC2} is switched from either the main battery or AC power if available. In this configuration all internal components which utilize V_{CC0} power plane only when V_{CC1} is absent. Normally (when VCC1_PWRGD is asserted) they are switched internally to the VCC1 power plane.

TABLE 5 - POWER COMSUMPTION IN VARIOUS STATES

V_{CC2} (VDC)	V_{CC1} (VDC)	8051 STATE	CLOCK STATE	SYM	TYP	MAX	COMMENTS
3.3	3.3	Run	24 MHz	I_{CC2} I_{CC1}	15 ma 24 ma	20 ma 30 ma	FLOPPY @ 1 Meg Data Rate I2C @ 24 MHz
3.3	3.3	Run	12 MHz	I_{CC2} I_{CC1}	13 ma 12 ma	15 ma 18 ma	Floppy @ 500K Data Rate I2C @ 12 MHz
3.3	3.3	Run	Ring OSC	I_{CC2} I_{CC1}	>1ma 8 ma	2 ma 10 ma	PLL On I2C Off
3.3	3.3	Idle	Ring OSC	I_{CC2} I_{CC1}	>1ma 5 ma	2 ma 7 ma	PLL Off
0	3.3	Run	Ring OSC	I_{CC2} I_{CC1}	 8 ma	 10 ma	PLL Off I2C Off
0	3.3	Idle	Ring OSC	I_{CC2} I_{CC1}	 6 ma	 8 ma	PLL Off I2C Off
0	3.3	Sleep	Stop	I_{CC1}		160 µa	XOSEL=1
0	3.3	Sleep	Stop	I_{CC1}	5 µa	10 µa	XOSEL=0
0	0			I_{CC0}	40 µa	60 µa	$2.4 < V_{cc0} < 4$ VDC, XOSEL=1,
0	0			I_{CC0}	0.4 µa	1.5 µa	$2.4 < V_{cc0} < 4$ VDC, XOSEL = 0

Note: When a single-ended 32.768kHz clock source is selected (see Section 32kHz Clock Input). The FDC37N972 uses the XOSEL pin to select either a 32.768kHz input clock or a 32.768kHz crystal to drive the Real Time Clock Interface (Table 2 - PIN FUNCTION DESCRIPTION). When XOSEL = '0', The RTC uses a 32.768kHz crystal connected between the XTAL1 and XTAL2 pins. When XOSEL = '1', the RTC is driven by a 32.768kHz single-ended clock source connected to the XTAL2 pin.

TABLE 7 - POWER PIN LIST

BIAS PINS		
156	VCC0	RTC (V_{BAT})Supply Voltage 2.7-3.3V ibat<2ma
29, 143, 176	VCC1	8051 + AB + CI + RTC+ ACPI + PM1 + WDT + MR + CR + PM + AB2 + FI + PWM + KI + GPIO + LED + IR + 3.3V +/-5% Supply Voltage (Note)
83, 104, 120, 205	VCC2	SR + PCG + FDC + DDS + UART + PP + PS/2 + Core +3.3V +/-5%Supply Voltage
160	AGND	Analog Ground for VCC0.
1, 7, 49, 73, 89, 107, 132, 167, 192	VSS	Digital Ground

Note:

AB	= ACCESS.bus	KI	= Keyboard Interface
CI	= Control Inputs	GPIO	= General Purpose I/O Interface
WDT	= Watch Dog Timer	IR	= Infrared
MR	= Mailbox Registers	SR	= System Reset
CR	= Control Registers	PCG	= PLL Clock Generator
PM	= Power Management	FDC	= Floppy Disk Controller
AB2	= ACCESS.BUS2	DDS	= Digital Data Seperator
FI	= Flash Interface	PP	= Multi-Mode Parallel Port

PWRGD and VCC1_PWRGD timing is illustrated in **FIGURE 3** through **FIGURE 5**.

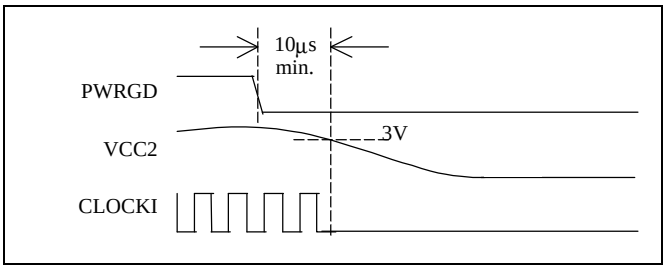


FIGURE 3 – POWER-FAIL EVENT

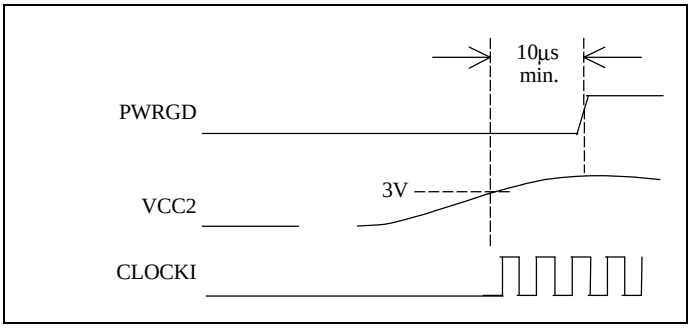


FIGURE 4 - VCC2 POWER-UP TIMING

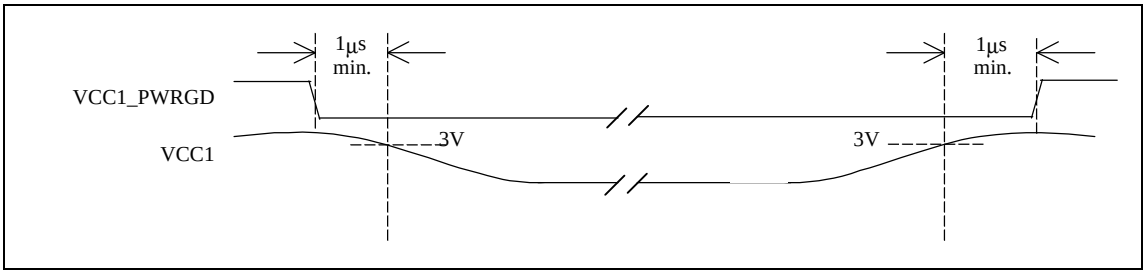


FIGURE 5 - VCC1_PWRGD TIMING

These figures also appear in the "Timing Diagrams" section of this spec.

FUNCTIONAL DESCRIPTION

FDC37N972 OPERATING REGISTERS

The address map, shown below in TABLE 8, shows the set of operating registers and addresses for each of the logical blocks of the FDC37N972 Ultra I/O controller. The base addresses of the FDC, Parallel, Serial 1 and Infrared ports can be moved via the configuration registers.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37N972 through a series of read/write registers. The range of base I/O port addresses for these registers is shown in TABLE 8. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits. Most of the registers support zero wait-state access (NOWS). All host interface output buffers are capable of sinking a minimum of 6 mA.

TABLE 8 - FDC37N972 OPERATING REGISTER ADDRESSES

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	BASE I/O RANGE (NOTE3)	FIXED BASE OFFSETS	ISA CYCLE TYPE
0x00	FDC	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TSR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR	NOWS
0x03	Parallel Port	[0x100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x100:0x0FF8] ON 8 BYTE BOUNDARIES (all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+0 : Data / ecpAfifo +1 : Status +2 : Control +400h : cfifo / ecpDfifo tfifo / cnfgA +401h : cnfgB +402h : ecr	Std. ISA I/O

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	BASE I/O RANGE (NOTE3)	FIXED BASE OFFSETS	ISA CYCLE TYPE
0x04	Serial Port 1	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB | LSB div +1 : IER | MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR	NOWS
0x05	Infrared Port	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB | LSB div +1 : IER | MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR	NOWS
	0x62, 0x63	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Register Block N, address 0 +1 : Register Block N, address 1 +2 : Register Block N, address 2 +3 : Register Block N, address 3 +4 : Register Block N, address 4 +5 : Register Block N, address 5 +6 : Register Block N, address 6 +7 : SCE Master Control Reg.	
0x06	RTC	Not Relocatable Fixed Base Address	0x70, 0x74 : Address Register 0x71, 0x76 : Data Register	NOWS Std. ISA I/O
0x07	KYBD	Not Relocatable Fixed Base Address	0x60 : Data Register 0x64 : Command/Status Reg.	NOWS

Note 1: Refer to the configuration register descriptions for setting the base address
Note 2: This chip uses all ISA address bits to decode the base address of each of its logical devices.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the Floppy Disk Drives (FDD). The FDC integrates the functions of the formatter/controller, Digital Data Separator, Write Precompensation and data rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary FDC core.

FDC INTERNAL REGISTERS

The FDC contains eight internal registers, which facilitate the interfacing between the host microprocessor and the disk drive TABLE 9 shows the addresses required toaccess these registers. Registers other than the ones shown are not supported.

TABLE 9 - STATUS, DATA AND CONTROL REGISTERS

FDC PRIMARY BASE I/O ADDRESS OFFSET	R/W	REGISTER
0	R	Status Register A (SRA)
1	R	Status Register B (SRB)
2	R/W	Digital Output Register (DOR)
3	R/W	Tape Drive Register (TDR)
4	R	Main Status Register (MSR)
4	W	Data Rate Select Register (DSR)
5	R/W	Data (FIFO)
6		Reserved
7	R	Digital Input Register (DIR)
7	W	Configuration Control Register (CCR)

STATUS REGISTER A (SRA)

FDC I/O BASE ADDRESS + 0x00
(READ ONLY)

This register is read-only and monitors the state of the FDC Interrupt pin and several disk

interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of SRA.

TABLE 10 - SRB - PS/2 MODEL 30 MODE

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	N/A	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION
Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX
Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2
Active low status of the DRV2 disk interface input pin, indicating that a second drive has been installed.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

TABLE 11 - SRA - PS/2 MODEL 30 MODE

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	NHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the FDC's DRQ output pin.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

DIGITAL OUTPUT REGISTER (DOR)

FDC I/O BASE ADDRESS + 0X02 (READ/WRITE)

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

TABLE 12 - FDC DOR

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the two drive selects output pins nds0 and nds1, thereby allowing only one drive to be selected at one time.

BIT 2 nreset
A logic “0” written to this bit resets the FDC. This reset will remain active until a logic “1” is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN
PC/AT and Model 30 Mode: Writing this bit to logic “1” will enable the FDC’s ndack and TC inputs and enable the FDC’s DRQ and Interrupt outputs. This bit being a logic “0” will disable the FDC’s ndack and TC inputs, and hold the FDC’s DRQ and Interrupt outputs in a high impedance state. This bit is a logic “0” after a reset.
PS/2 Mode: In this mode the TC and the FDC’s DRQ, ndack, and Interrupt pins are always enabled. During a reset, the DRQ, ndack, TC, and Interrupt pins will remain enabled, but this bit will be cleared to a logic “0”.

BIT 4 MOTOR ENABLE 0
This bit controls the nmtr0 disk interface output. A logic “1” in this bit will cause the output pin to assert.

BIT 5 MOTOR ENABLE 1
This bit controls the nmtr1 disk interface output. A logic “1” in this bit will cause the output pin to assert.

BIT 6 MOTOR ENABLE 2
This bit controls the nmtr2 disk interface output. A logic “1” in this bit will cause the output pin to assert.

BIT 7 MOTOR ENABLE 3
This bit controls the nmtr3 disk interface output. A logic “1” in this bit will cause the output pin to assert.

TABLE 13 – FDC SRB – PS/2 MODEL 30 MODE

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

TABLE 14 - FDC DOR

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the two drive selects output pins nds0 and nds1, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET
A logic “0” written to this bit resets the FDC. This reset will remain active until a logic “1” is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN
PC/AT and Model 30 Mode:
Writing this bit to logic “1” will enable the FDC’s nDACK and TC inputs and enable the FDC’s DRQ and Interrupt outputs. This bit being a logic “0” will disable the FDC’s nDACK and TC inputs, and hold the FDC’s DRQ and Interrupt outputs in a high impedance state. This bit is a logic “0” after a reset.

PS/2 Mode: In this mode the TC and the FDC’s DRQ, and Interrupt pins are always enabled. During a reset, the DRQ, TC, and Interrupt pins will remain enabled, but this bit will be cleared to a logic “0”.

BIT 4 MOTOR ENABLE 0
This bit controls the disk interface output. A logic “1” in this bit will cause the output pin to assert.

BIT 5 MOTOR ENABLE 1
This bit controls the nMTR1 disk interface output. A logic “1” in this bit will cause the output pin to assert.

BIT 6 MOTOR ENABLE 2
This bit controls the nMTR2 disk interface output. A logic “1” in this bit will cause the output pin to assert.

BIT 7 MOTOR ENABLE 3
This bit controls the nMTR3 disk interface output. A logic “1” in this bit will cause the output pin to assert.

TABLE 13 – FDC INTERNAL 2 DRIVE DECODE – DRIVES 0 AND 1 SWAPPED

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	Nds1	Nds0	Nmtr1	Nmtr0
X	X	X	1	0	0	0	1	Nbit 4	Nbit 5
X	X	1	X	0	1	1	0	Nbit 4	Nbit 5
X	1	X	X	1	0	1	1	Nbit 4	Nbit 5
1	X	X	X	1	1	1	1	Nbit 4	Nbit 5
0	0	0	0	X	X	1	1	Nbit 4	Nbit 5

TAPE DRIVE REGISTER (TDR)

FDC I/O BASE ADDRESS + 0x03 (READ/WRITE)

This register is included for 82077 software compatability. The TDR is unaffected by a software reset. The improved data separator incorporates tape drive support and requires the Tape Select bits in the FDC Tape Drive register to identify which drive has been assigned to receive this support (see the following section).

NORMAL FLOPPY MODE

Normal mode. The TDR allows the user to assign tape support to a particular drive during initialization. Any future references to that drive number automatically invokes tape support. The Tape Select bits are TDR[1:0]. The TDR Register contains only bits 0 and 1. When this register is read, bits 2 – 7 are a high impedance.

TABLE 14 - FDC TDR NORMAL FLOPPY MODE

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tape sel 1	tape sel 0

TAPE SEL1 (TDR.1)	TAPE SEL2 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

ENHANCED FLOPPY MODE 2 (OS2)

The TDR Register for Enhanced Floppy Mode 2 operation.

TABLE 15 - FDC TDR ENHANCED FLOPPY MODE 2 (OS2)

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	1	1	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

BIT 7 This bit is always set active high

BIT 6 This bit is always set active high

BITS 5 and 4 Drive Type ID
These bits reflect two of the bits of L0-CRF1 (Logical Device 0 – Configuration Register 0xF1). Which two bits these are depends on the last drive selected in the Digital Output Register. (See **TABLE 20**)

BITS 3 and 2 Floppy Boot Drive
These bits reflect two of the bits of L0-CRF1. Bit 3 = L0-CRF1-B7. Bit 2 = L0-CRF1-B6.

BIT 1 and 0 – Tape Drive Select (READ/WRITE)
Same as in Normal and Enhanced Floppy Mode 2.

TABLE 16 – DRIVE TYPE ID

DIGITAL OUTPUT REGISTER		**TDR REGISTER – DRIVE TYPE ID**	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	L0-CRF2 – B1	L0-CRF2 – B0
0	1	L0-CRF2 – B3	L0-CRF2 – B2
1	0	L0-CRF2 – B5	L0-CRF2 – B4
1	1	L0-CRF2 – B7	L0-CRF2 – B6

Note: L0-CRF2-Bx = Logical Device 0, Configuration Register F2, Bit x.

MID[1:0] FDD INTERFACE PINS
The FDC Media ID pins are not supported in the FDC37N972. The MID[1:0] inputs to the FDC core are strapped so that the Media ID bits the TDR are always “high”.

DATA RATE SELECT REGISTER (DSR)

FDC I/O BASE ADDRESS + 0x04 (WRITE ONLY)

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

TABLE 17 - FDC DSR

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See **TABLE 19** for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset and are set to 250 Kbps after a hardware reset.

BITS 2 - 4 PRECOMPENSATION SELECT
These three bits select the value of write precompensation that will be applied to the WDATA output signal. **TABLE 18** shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. This starting track number can be changed by the configure command.

BIT 5 UNDEFINED
Should be written as a logic "0".

BIT 6 LOW POWER
A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET
This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

TABLE 18 - FDC PRECOMPENSATION DELAYS

PRECOMP 432	PRECOMPENSATION DELAY (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default

Default: See **TABLE 16**

TABLE 19 – FDC DATA RATES

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	**DRT0**	**SEL1**	**SEL0**	**MFM**	**FM**		**1**	**0**
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: The DRATE and DENSEL values are mapped onto the DRIVEDEN pins.

TABLE 20 - FDC DRVDEN MAPPING

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

TABLE 21 - FDC DEFAULT PRECOMPENSATION DELAYS

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

MAIN STATUS REGISTER

FDC I/O BASE ADDRESS + 0x04
(READ ONLY)

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

TABLE 22 - FDC MSR

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY

BIT 0 - 3 DRVx BUSY
These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY
This bit is set to a “1” when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a “0” after the last command byte.

BIT 5 NON-DMA
This mode is selected in the SPECIFY command and will be set to a “1” during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO
Indicates the direction of a data transfer once a RQM is set. A “1” indicates a read and a “0” indicates a write is required.

BIT 7 RQM
Indicates that the host can transfer data if set to a “1”. No access is permitted if set to a “0”.

DATA REGISTER (FIFO)

FDC I/O BASE ADDRESS + 0x05 (READ/WRITE)

All command parameter information, disk data and result status are transferred between the host processor and the FDC through the Data Register. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error.

TABLE 31 gives several examples of the delays with a FIFO. The data is based upon the following formula:

Threshold # x [8/DATA RATE] - 1.5ms = Delay

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

TABLE 23 - FIFO SERVICE DELAY

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps* DATA RATE
1 byte	1 x 4 ms - 1.5 ms = 2.5 ms
2 bytes	2 x 4 ms - 1.5 ms = 6.5 ms
8 bytes	8 x 4 ms - 1.5 ms = 30.5 ms
15 bytes	15 x 4 ms - 1.5 ms = 58.5 ms

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 ms - 1.5 ms = 6.5 ms
2 bytes	2 x 8 ms - 1.5 ms = 14.5 ms
8 bytes	8 x 8 ms - 1.5 ms = 62.5 ms
15 bytes	15 x 8 ms - 1.5 ms = 118.5 ms

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 ms - 1.5 ms = 14.5 ms
2 bytes	2 x 16 ms - 1.5 ms = 30.5 ms
8 bytes	8 x 16 ms - 1.5 ms = 126.5 ms
15 bytes	15 x 16 ms - 1.5 ms = 238.5 ms

DIGITAL INPUT REGISTER (DIR)

FDC I/O BASE ADDRESS + 0X07 (READ ONLY)

This register is read-only in all modes.

DIR - PC-AT Mode

TABLE 24 - FDC DIR ALL MODES

	7	6	5	4	3	2	1	0
	DSK CHG							
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 – 6 UNDEFINED
The data bus outputs D0 – 6 will remain in a high impedance state during a read of this register.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

DIR – PS/2 MODE

TABLE 25 - FDC DIR PS/2 MODE

	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESET COND.	DSK CHG N/A	1 N/A	1 N/A	1 N/A	1 N/A	DRATE SEL1 N/A	DRATE SEL0 N/A	nHIGH DENS 1

BIT 0 nhigh DENS
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 – 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See **TABLE 19**for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 – 6 UNDEFINED
Always read as a logic “1”

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

DIR – MODEL 30 MODE

TABLE 26 - FDC DIR MODEL 30 MODE

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	nOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 and 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See **TABLE 19** for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset and are set to 250 Kbps after a hardware reset.

BIT 2 nOPREC
This bit reflects the value of nOPREC bit set in the CCR register.

BIT 3 DMAEN
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED
Always read as a logic "0"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the pin.

CONFIGURATION CONTROL REGISTER (CCR)

FDC I/O BASE ADDRESS + 0x07
(WRITE ONLY)

TABLE 27 - FDC CCR PC/AT AND PS/2 MODE

	7	6	5	4	3	2	1	0
							DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See **TABLE 19** for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0"

TABLE 28 - FDC CCR - PS/2 MODEL 30 MODE

	7	6	5	4	3	2	1	0
						NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See **TABLE 19** for the appropriate values.

BIT 2 NO PRECOMPENSATION
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED
Should be set to a logical "0". **TABLE 19** shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

TABLE 29 - FDC STATUS REGISTER 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: Step pulses in the Recalibrate command. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

TABLE 30 - FDC STATUS REGISTER 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: Read Data, Read Deleted Data command - the FDC did not find the specified sector. Read ID command - the FDC cannot read the ID field without an error. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

TABLE 31 - FDC STATUS REGISTER 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

TABLE 32 - FDC STATUS REGISTER 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			UNUSED. THIS BIT IS ALWAYS "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the nDS1, nDS0 pins.

FDC RESET

There are three sources of system reset on the FDC: the nRESET_OUT bit of the 8051's Output enable Register (which controls the nRESET_OUT pin of the FDC37N972); a reset generated via a bit in the DOR; and a reset generated via a bit in the DSR. At VCC2 power on, a VCC2 Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a RESET, and the Floppy Disk Controller enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the Floppy Disk Controller waits for a new command. Drive polling will start unless disabled by a new Configure command.

nRESET_OUT PIN (HARDWARE RESET)
The nRESET_OUT pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR RESET VS. DSR RESET (SOFTWARE RESET)
These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a nRESET_OUT pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

FDC MODES OF OPERATION

The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of IDENT and MFM, bits[3] and [2] respectively of L0-CRF0.

PC/AT MODE - (IDENT high, MFM a "don't care")
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (The FDC's IRQ and DRQ can be hi-Z), and TC and DENSEL become active high signals.

PS/2 MODE - (IDENT low, MFM high)
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care", (the FDC's IRQ and DRQ are always valid), TC and DENSEL become active low.

MODEL 30 MODE - (IDENT low, MFM low)
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (The FDC's IRQ and DRQ can be hi-Z), TC is active high and DENSEL is active low.

DMA TRANSFERS

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating its DRQ pin during a data transfer command. The FIFO is enabled directly by asserting nDACK and addresses need not be valid.

Note that if the DMA controller (i.e. 8237A) is programmed to function in verify mode, a pseudo read is performed by the FDC based only on nDACK. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled, the FDC can perform the above operation by using the Verify command; no DMA operation is needed.

CONTROLLER PHASES

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

COMMAND PHASE

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to **TABLE 33** for the command set descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received

byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

EXECUTION PHASE

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by an FDC IRQ or DRQ depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The FDC's IRQ pin and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The FDC's IRQ pin can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the FDC's IRQ pin and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The FDC's IRQ pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The FDC's IRQ pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FDC's IRQ pin will also be deactivated if TC and nDACK both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC activates the FDC's DRQ pin when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the FDC's DRQ pin when the FIFO becomes empty. FDC's DRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nDACK). A data underrun may

occur if the FDC's DRQ is not removed in time to prevent an unwanted cycle.

DMA Mode - Transfers from the Host to the FIFO

The FDC activates the FDC's DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the nDACK and nIOW pins placing data in the FIFO. The FDC's DRQ remains active until the FIFO becomes full. The FDC's DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will also deactivate the FDC's DRQ pin when TC becomes true (qualified by nDACK), indicating that no more data is required. The FDC's DRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOW of the last byte, if no edge is present on nDACK). A data overrun may occur if the FDC's DRQ is not removed in time to prevent an unwanted cycle.
Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

RESULT PHASE

The generation of the FDC's IRQ determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds withthe command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 33 for explanations of the various symbols used. TABLE 34 lists the required parameters and the results associated with each command that the FDC is capable of performing.

TABLE 33 - DESCRIPTION OF THE FDC COMMAND SYMBOLS

<table>
<tr><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>C</td><td>Cylinder Address</td><td>The currently selected address; 0 to 255.</td></tr>
<tr><td>D</td><td>Data Pattern</td><td>The pattern to be written in each sector data field during formatting.</td></tr>
<tr><td>D0, D1, D2, D3</td><td>Drive Select 0-3</td><td>Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.</td></tr>
<tr><td>DIR</td><td>Direction Control</td><td>If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.</td></tr>
<tr><td>DS0, DS1</td><td>Disk Drive Select</td><td><table><tr><th>DS1</th><th>DS0</th><th>DRIVE</th></tr><tr><td>0</td><td>0</td><td>drive 0</td></tr><tr><td>0</td><td>1</td><td>drive 1</td></tr><tr><td>1</td><td>0</td><td>drive 2</td></tr><tr><td>1</td><td>1</td><td>drive 3</td></tr></table></td></tr>
<tr><td>DTL</td><td>Special Sector Size</td><td>By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.</td></tr>
<tr><td>EC</td><td>Enable Count</td><td>When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).</td></tr>
<tr><td>EFIFO</td><td>Enable FIFO</td><td>This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).</td></tr>
<tr><td>EIS</td><td>Enable Implied Seek</td><td>When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.</td></tr>
<tr><td>EOT</td><td>End of Track</td><td>The final sector number of the current track.</td></tr>
<tr><td>GAP</td><td></td><td>Alters Gap 2 length when using Perpendicular Mode.</td></tr>
<tr><td>GPL</td><td>Gap Length</td><td>The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).</td></tr>
<tr><td>H/HDS</td><td>Head Address</td><td>Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.</td></tr>
<tr><td>HLT</td><td>Head Load Time</td><td>The time interval that the FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.</td></tr>
</table>

SYMBOL	NAME	DESCRIPTION
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either tha DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. **N SECTOR SIZE** 128 bytes 256 bytes 512 bytes 1024 bytes ... ... 07 16 Kbytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode, interfacing to a DMA controller by means of the DRQ and nDACK signals.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.

SYMBOL	NAME	DESCRIPTION
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

FDC INSTRUCTION SET

TABLE 34 - FDC INSTRUCTION SET

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

WRITE DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
Execution										Data transfer between the FDD and system.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

READ A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------- DTL -------								
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

VERIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	-------- C --------								Sector ID information prior to Command execution.
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								
	W	------- EOT -------								
	W	------- GPL -------								
	W	------ DTL/SC ------								
Execution										No data transfer takes place.
Result	R	------- ST0 -------								Status information after Command execution.
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	-------- C --------								Sector ID information after Command execution.
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

VERSION										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller
FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	-------- N --------								Bytes/Sector
	W	-------- SC --------								Sectors/Cylinder
	W	------- GPL -------								Gap 3
	W	-------- D --------								Filler Byte
Execution for Each Sector Repeat:	W	-------- C --------								Input Sector Parameters
	W	-------- H --------								
	W	-------- R --------								
	W	-------- N --------								FDC formats an entire cylinder
Result	R	------- ST0 -------								Status information after Command execution
	R	------- ST1 -------								
	R	------- ST2 -------								
	R	------ Undefined ------								
	R	------ Undefined ------								
	R	------ Undefined ------								
	R	------ Undefined ------								

RECALIBRATE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	------- ST0 -------								Status information at the end of each seek operation.
	R	------- PCN -------								

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	--- SRT ---				--- HUT ---				
	W	------ HLT ------							ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	------- ST3 -------								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	------- NCN -------								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	--- FIFOTHR ---				
Execution	W	--------- PRETRK ---------								

RELATIVE SEEK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	------- RCN -------								

DUMPREG										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	------ PCN-Drive 0 -------								
	R	------ PCN-Drive 1 -------								
	R	------ PCN-Drive 2 -------								
	R	------ PCN-Drive 3 -------								
	R	---- SRT ----				--- HUT ---				
	R	------- HLT -------							ND	
	R	------- SC/EOT -------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	-- FIFOTHR --				
	R	-------- PRETRK --------								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	-------- ST0 --------								Status information after Command execution.
										Disk status after the Command has completed
	R	-------- ST1 --------								
	R	-------- ST2 --------								
	R	-------- C --------								
	R	-------- H --------								
	R	-------- R --------								
	R	-------- N --------								

PERPENDICULAR MODE									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	----- Invalid Codes -----								Invalid Command Codes (NoOp - FDC goes into Standby State)
Result	R	------- ST0 -------								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

FDC DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

TABLE 35 - FDC SECTOR SIZES

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

READ DATA

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see **TABLE 35** above). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command. After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. Ifa CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command.

TABLE 40 - VERIFY COMMAND RESULT PHASE TABLE describes the effect of the SK bit on the Read Data command execution and results. Except where noted in **TABLE 36**, the C or R value of the sector address is automatically incremented (see **TABLE 42**).

TABLE 36 - EFFECTS OF MT AND N BITS

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

TABLE 37 - SKIP BIT VS READ DATA COMMAND

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped")

READ DELETED DATA

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

TABLE 41 describes the effect of the SK bit on the Read Deleted Data command execution and results. Except where noted in **TABLE 41**, the C or R value of the sector address is automatically incremented (see**TABLE 42**).

TABLE 38 - SKIP BIT VS. READ DELETED DATA COMMAND

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for
0	Deleted Data	Yes	No	Normal termination
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped")
1	Deleted Data	Yes	No	Normal termination

READ A TRACK

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

TABLE 39 - RESULT PHASE TABLE

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

WRITE DATA

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

Transfer Capacity

EN (End of Cylinder) bit
ND (No Data) bit
Head Load, Unload Time Interval
ID information when the host terminates the command
Definition of DTL when N = 0 and when N does not = 0.

WRITE DELETED DATA

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

VERIFY

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, TC (pin 94) cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to TABLE 42 and TABLE 43 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

TABLE 40 - VERIFY COMMAND RESULT PHASE TABLE

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT ≤ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

FORMAT A TRACK

The Format command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the IDX pin again and it terminates the command.

TABLE 45 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

TABLE 41 - DISKETTE FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM		DATA	CRC	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE						22x 4E	12x 00	3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM	DATA	CRC	GAP3	GAP 4b
40x FF	6x 00	FC	26x FF	6x 00	FE						11x FF	6x 00	FB or F8				

PERPENDICULAR FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM		DATA	CRC	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE						41x 4E	12x 00	3x A1	FB F8				

TABLE 42 - TYPICAL VALUES FOR FORMATTING

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.
NOTE: All values except sector size are in hex.

FDC CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

READ ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

RECALIBRATE

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter

and checks the status of the nTR0 pin from the FDD. As long as the nTR0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTR0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTR0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once.

Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

SEEK

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once. Note that if implied seek is not enabled, the read and write commands should be preceded by:

Seek command - Step to the proper track
Sense Interrupt Status command - Terminate the Seek command
Read ID - Verify head is on proper track
Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command be issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

SENSE INTERRUPT STATUS

An interrupt signal on the FDC's IRQ pin is generated by the FDC for one of the following reasons:

Upon entering the Result Phase of:
Read Data command
Read A Track command
Read ID command
Read Deleted Data command
Write Data command
Format A Track command
Write Deleted Data command
Verify command
End of Seek, Relative Seek, or Recalibrate command

FDC requires a data transfer during the execution phase in the non-DMA mode The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

TABLE 43 - INTERRUPT IDENTIFICATION

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

SENSE DRIVE STATUS

Sense Drive Status obtains drive status information. It has no execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

SPECIFY

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in TABLE 44 - Drive Control Delays (ms). The values are the same for MFM and FM.

TABLE 44 - DRIVE CONTROL DELAYS(MS)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the FDC's DRQ pin. Non-DMA mode uses the RQM bit and the FDC's IRQ pin to signal data transfers.

CONFIGURE

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

VERSION

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

RELATIVE SEEK

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR	ACTION
0	Step Head Out
1	Step Head In

DIR Head Step Direction Control

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number. The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

PERPENDICULAR MODE

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. TABLE 54 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0). It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive will be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1". If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

TABLE 45 - EFFECTS OF WGATE AND GAP BITS

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used. The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

ENHANCED DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command contains the data from these two commands.

COMPATIBILITY

The FDC37N972 was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, FDC subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

PARALLEL PORT FDC

Refer to the Parallel Port Section for details.

HOT SWAPPABLE FDD CAPABILITY

The FDC output pins will tri-state whenever the FDC Logical Device is powered-down or not activated. In addition setting bit 7 of the FDD Mode Configuration register (LD0_CRF0) will tri-state the FDC output pins. Bit 7 only affects the standard FDC interface, it has no effect on the Parallel Port Floppy Interface.

The following table illustrates the state of the FDC and Parallel Port FDC pins for combinations of 1) the FDC Output Control bit; 2) the Activate bit; and 3) the FDC powerdown state.

TABLE - 46 FDC HOT SWAPPING STATE OF THE FDC AND PARALLEL PORT FDC PINS

FDD MODE REGISTER, BIT[7]	ACTIVATE BIT	FDC IN POWER DOWN	FDC PINS	PARALLEL PORT FDC PINS
X	0	X	Hi-Z	Hi-Z
X	1	Y	Hi-Z	Hi-Z
0	1	N	Active	Active
1	1	N	Hi-Z	Active

When the FDC is disabled, powered down or inactive the FDC output pins will tri-state allowing 'hot-swapping' of the Floppy Disk Drive. The following table lists the five control/configuration mechanisms that power down or deactivate the FDC logical device.

TABLE 47 - FDC HOT SWAPPING MECHANISMS

MECHANISM	FDC OUTPUT PINS STATE				
	Tri-State	Tri-State	Tri-State	Tri-State (Note 1)	Tri-State (Note 2)
FDC Logical Dev Activate bit =0: FDC LD deactivated =1: FDC LD activated Refer to the description of the FDC Logical Device Configuration register 0x30 in the Configuration section of the FDC37N972 Specification.	0	X	1	1	1
FDC Logical Dev Base Address 0x100 ≤ Base ≤ 0x0FF8: FDC LD Base Address Valid. 0xFFF < Base < 0x100: FDC LD Base Address Invalid. Refer to the description of the FDC Base I/O Address registers in the Configuration section of the FDC37N972 Specification.	X	INVALID BASE ADDRESS	VALID BASE ADDRESS	VALID BASE ADDRESS	VALID BASE ADDRESS
GCR 0x22 bit-0 (FDC Power) =0: Power Off =1: Power On Refer to the description of the Global Config Register 0x22 in the Configuration section of the FDC37N972 Specification.	X	X	0	1	1
DSR, bit-6 (pwr down) =0: Normal Run =1: Manual Pwr down Refer to the description of the DSR in the FDC section of any SMSC Super or Ultra I/O data sheet.	X	X	X	1	0

MECHANISM	FDC OUTPUT PINS STATE				
GCR 0x23 bit-0 (FDC auto power management) =1: Pwr Mngnt on =0: Pwr Mngnt off Refer to the description of the Global Config Register 0x23 in the Configuration section of the FDC37N972 Specification.	X	X	X	X	1

Note: FDC Output pins = nWDATA, DRVDEN0, nHDSELm nWGATE, nDIR, nSTEP, nDS1, nDS0, nMTR0, nMTR1.

Note1: DSR pwr down overrides auto pwr down.

Note 2: Outputs tri-state only if all of the required auto power down conditions are met, otherwise outputs are active. See Auto Power Management Section of the FDC37C93x Data Sheet.

FDC FORCE WRITE PROTECT

The FDC37N972 includes a Force Write Protect function for the floppy disk controller. Force Write Protect asserts the internal nWRTPRT input to the controller (**TABLE 48** and FIGURE **6**).

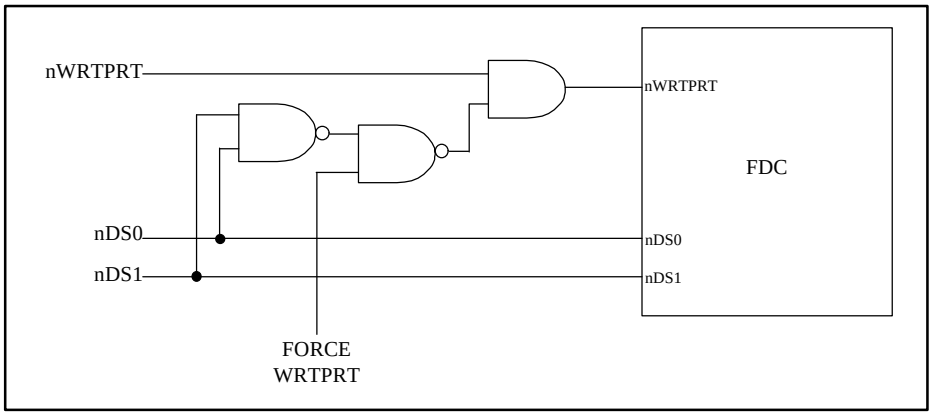


FIGURE 6 - FORCE WRITE PROTECT FUNCTION

NOTE: This figure is for illustration purposes only and is not intended to suggest specific implementation details.

The FORCE WRTPRT bit is D0 in the Disable register (see Section **Disable** *REGISTER* on page 166). The FORCE WRTPRT bit is active-high and set to “0” by default. The Force Write Protect function applies to the nWRTPRT input from the FDD Interface as well as the nWRTPRT input from the Parallel Port FDC.

TABLE 48 - FORCE WRTPRT FUNCTION

nWRTPRT (FDD PIN)	FORCE WRTPRT	nDS0	nDS1	nWRTPRT (FDC)	DESCRIPTION
0	X	X	X	0	Active nWRTPRT pin function is always enabled.
1	1	1	1	1	nWRTPRT function inactive.
1	0	1	1	1	
1	1	0	1	0	Enabled FORCE WRTPRT function overrides an inactive nWRTPRT pin.
1	1	1	0	0	

ACPI EMBEDDED CONTROLLER

Overview

ACPI defines a standard hardware and software communications interface between the OS and an embedded controller. This interface allows the OS to support a standard driver that can directly communicate with the embedded controller, allowing other drivers within the system to communicate with and use the EC resources; for example, Smart Battery and AML code.

The FDC37N972 contains an Embedded Controller Interface (ECI) to handle SCI Wake and Run-time event processing (FIGURE **8**). The ECI is configured in Logical Device Number 8 in the FDC37N972 configuration register map and presents an 8042-style interface to the ISA host.

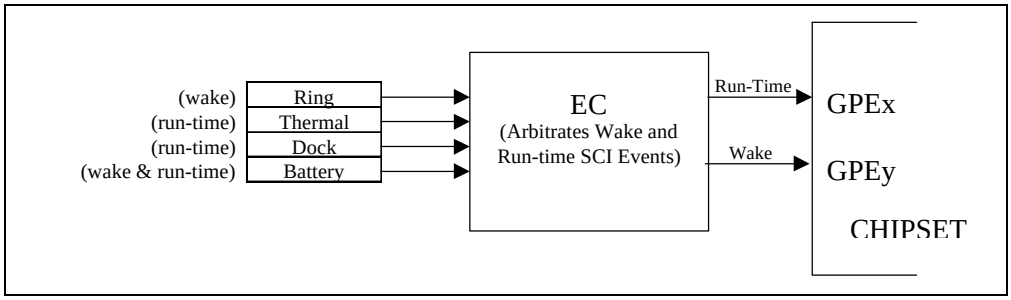


FIGURE 7 – EMBEDDED CONTROL (EC) ILLUSTRATION

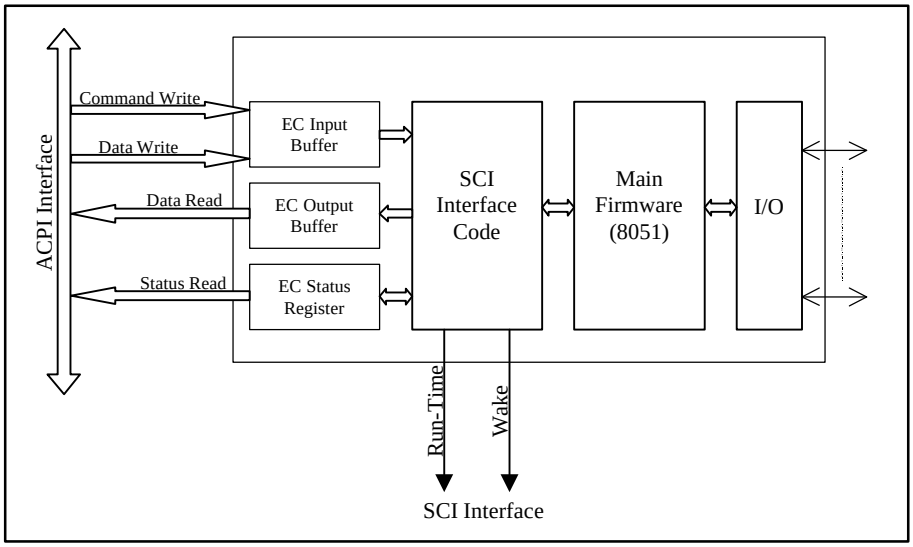


FIGURE 8 – GENERIC ACPI EC BLOCK DIAGRAM

ECI CONFIGURATION REGISTERS

The three device configuration registers in LDN8 provide ECI activation control and the base address for the ECI run-time registers (TABLE 49). Register 0x30 is the Activate register. The Activate register qualifies address decoding for the ECI; e.g., if the Activate bit D0 in the Activate register is "0", ECI addresses will not be decoded; if the Activate bit is "1", ECI addresses will be decoded depending on the values programmed in the ECI Primary Base Address registers. Registers 0x60 and 0x61 are the ECI Primary Base Address registers. Register 0x60 is the ECI Primary Base Address High Byte, register 0x61 is the ECI Primary Base Address Low Byte.

NOTE: Bits D0 and D2 in the ECI Primary Base Address Low Byte must be "0". For example, 0x62 is a valid ECI Base Address, while 0x66 is not a valid ECI Base Address. The valid ECI Primary Base Address range is 0x0000 – 0x0FFA.

TABLE 49 - ECI CONFIGURATION REGISTERS (LDN8)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1& VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	ACTIVATE							
						Reserved							Activate
0x60	R/W	0x00	0x00	0x00	-	ECI PRIMARY BASE ADDRESS HIGH BYTE							
0x61	R/W	0x62	0x62	0x62	-	ECI PRIMARY BASE ADDRESS LOW BYTE[1]							
						A7	A6	A5	A4	A3	"0"	A1	"0"

NOTE[1] Bits D0 and D2 of the ECI Base Address Low Byte must be "0".

ECI RUNTIME REGISTERS

An ACPI-compliant ECI contains three registers: EC_COMMAND, EC_STATUS, and EC_DATA. The ECI registers occupy two addresses in the Host I/O space (TABLE 50).

The EC_DATA and EC_COMMAND registers appear as a single 8-bit data register in the 8051. The CMD bit in the EC_STATUS register is used by the 8051 to discriminate commands from data written by the host to the ECI. CMD is controlled by hardware: host writes to the EC_DATA register set CMD = "0"; host writes to the EC_COMMAND register set CMD = "1".

Descriptions of these registers follow in the sections below.

TABLE 50 - ECI RUN-TIME REGISTERS

	ISA HOST INTERFACE		8051 INTERFACE					
REGISTER NAME	**HOST INDEX**	**HOST TYPE**	**CMD[1]**	**8051 INDEX (7F00+)**	**8051 TYPE**	**POWER PLANE**	**VCC1 POR**	**VCC2 POR**
EC_DATA	ECI Base Address	R/W	0	0x53	R/W	VCC1	-	-
EC_COMMAND	ECI Base Address + 4	W	1	0x53	R	VCC1	-	-
EC_STATUS	ECI Base Address + 4	R	-	0x54	R/W	VCC1	0x00	-

NOTE[1] CMD is bit D3 in the EC_STATUS register.

EC_STATUS REGISTER

The EC_STATUS register indicates the state of the Embedded Controller Interface. To the host, the EC_STATUS register is read-only. To the 8051, some bits in the EC_STATUS register are read-only (TABLE 51). These bits are controlled by hardware. The 8051 software controlled bits in the EC_STATUS register are read/write.

TABLE 51 – EC_STATUS REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R**	**R/W**	**R**	**R**
NAME	UD[1]	SMI_EVT	SCI_EVT	BURST	CMD	UD[1]	IBF	OBF

NOTE[1] The UD bits are User-Defined. UD bits are maintained by 8051 software, only.

OBF Bit – D0
The Output Buffer Full (OBF) flag is set when the 8051 writes a byte of data into the data port (EC_DATA), but the host has not yet read it.

Once the host reads the status byte and sees the OBF flag set, the host reads the data port to get the byte of data that the 8051 has written.

Once the host reads the data, the OBF flag is automatically cleared by hardware. An EC_OBF interrupt signals the 8051 that the data has been read by the host and the 8051 is free to write more data to the EC_DATA register.

The EC_OBF interrupt is generated whenever the OBF bit in the EC_STATUS register is reset.

The EC_OBF interrupt is routed to bit 3 in the INT0 SRC register (FIGURE 19). The EC_OBF interrupt mask is bit 4 in the INT1 Mask register.

IBF Bit – D1
The Input Buffer Full (IBF) flag is set when the host has written a byte of data to the command or data port, but the 8051 has not yet read it.

An EC_IBF interrupt signals the 8051 that there is data available. Once the 8051 reads the status byte and sees the IBF flag set, the 8051 reads the data port to get the byte of data that the host has written.

Once the 8051 reads the data, the IBF flag is automatically cleared by hardware. The 8051 must then generate a software interrupt (SCI) to

alert the host that the data has been read and that the host is free to write more data to the ECI as needed.

An EC_IBF interrupt is generated whenever the IBF bit in the EC_STATUS register is set. The EC_IBF interrupt is routed to bit 4 in the INT0 SRC register. The EC_IBF interrupt mask is bit 5 in the INT1 Mask register.

CMD Bit – D3

The CMD bit is "1" when the EC_DATA register contains a command byte; the CMD bit is "0" when the EC_DATA register contains a data byte.

The CMD bit is controlled by hardware: host writes to the EC_DATA register set CMD = "0"; host writes to the EC_COMMAND register set CMD = "1".

The CMD bit allows the embedded controller to differentiate the start of a command sequence from a data byte write operation.

BURST Bit – D4

The BURST bit is "1" when the EC is in Burst Mode for polled command processing; the BURST bit is "0" when the EC is in Normal Mode for interrupt-driven command processing.

The BURST bit is an 8051-maintained software flag that indicates the embedded controller has received the Burst Enable command from the host, has halted normal processing, and is waiting for a series of commands to be sent from the host. Burst Mode allows the OS or system management handler to quickly read and write several bytes of data at a time without the overhead of SCIs between commands.

SCI_EVT Bit – D5

The SCI Event flag SCI_EVT is "1" when an SCI event is pending; i.e., the 8051 is requesting an SCI query; SCI_EVT is "0" when no SCI events are pending.

The SCI_EVT bit is an 8051-maintained software flag that is set when the embedded controller has detected an internal event that requires operating system attention. The EC sets SCI_EVT before generating an SCI to the OS.

SMI_EVT Bit – D6

The SMI Event flag SMI_EVT is "1" when an SMI event is pending; i.e., the 8051 is requesting an SMI query; SMI_EVT is "0" when no SMI events are pending.

The SMI_EVT bit is an 8051-maintained software flag that is set when the embedded controller has detected an internal event that requires system management interrupt handler attention. The EC sets SMI_EVT before generating an SMI.

EC_COMMAND Register

The EC_COMMAND register is a write-only register that allows the host to issue commands to the embedded controller.

Writes to the EC_COMMAND register are latched in the 8051 data register and the input buffer full flag is set in the EC_STATUS register. Writes to the EC_COMMAND register also cause the CMD bit to be set to "1" in the EC_STATUS register.

EC_DATA Register

The EC_DATA register is a read/write register that allows the host to issue command arguments to the embedded controller and allows the OS to read data returned by the embedded controller.

Host writes to the EC_DATA register are latched in the 8051 data register and the input buffer full flag is set in the EC_STATUS register. Host writes to the EC_DATA register also cause the

CMD bit to be reset to “0” in the EC_STATUS register.

Host reads from the EC_DATA register return data from the 8051 data register and clear the output buffer full flag in the EC_STATUS register.

SERIAL PORT (UART)

The FDC37N972 incorporates one full function UART. The UART is compatible with the NS16450, the 16450 ACE registers and the NSC16550A. The UART performs serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UART contains a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UART is also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UART. The interrupt from a UART is enabled by programming OUT2 of the UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt.

REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The FDC37N972 contains a serial port, which contains a register set as described below.

TABLE 52 - ADDRESSING THE SERIAL PORT

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write)

Note: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the FDC37N972 . All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

BIT 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

BIT 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

BIT 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

BIT 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

BITS 4 - 7
These bits are always logic "0".

FIFO CONTROL REGISTER (FCR)

Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported.

BIT 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

BIT 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to “0”. The shift register is not cleared. This bit is self-clearing.

BIT 2
Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to “0”. The shift register is not cleared. This bit is self-clearing.

BIT 3
Writing to this bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

BITS 4 and 5
Reserved

BITS 6 and 7
These bits are used to set the trigger level for the RCVR FIFO interrupt.

BIT 7	BIT 6	RCVR FIFO TRIGGER LEVEL (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

INTERRUPT IDENTIFICATION REGISTER (IIR)

Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist.

They are in descending order of priority:
1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

BIT 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

BITS 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

BIT 3
In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

BITS 4 and 5
These bits of the IIR are always logic "0".

BITS 6 and 7
These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

TABLE 53 - INTERRUPT CONTROL TABLE

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

LINE CONTROL REGISTER (LCR)

Address Offset = 3H, DLAB = 0, READ/WRITE

This register contains the format information of the serial line. The bit definitions are:

BITS 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

BIT 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

BIT 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).
BIT 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.
BIT 5
Stick Parity bit. When bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

BIT 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.
BIT 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)

Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

BIT 0
This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

BIT 1
This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

BIT 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

BIT 3
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

BIT 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:
1. The TXD is set to the Marking State(logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

BITS 5 - 7
These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

BIT 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

BIT 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

BIT 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

BIT 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

BIT 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status

Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time. Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

BIT 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

BIT 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty,

BIT 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

MODEM STATUS REGISTER (MSR)

Address Offset = 6H, DLAB = X, READ/WRITE This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information.

These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

BIT 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

BIT 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

BIT 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

BIT 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state. NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

BIT 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

BIT 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

BIT 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

BIT 7
This bit is the complement of the Data Carrier Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)

Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is the 24 MHz crystal divided by 13, giving a 1.8462 MHz clock.

TABLE 54 shows the baud rates possible with a 1.8462 MHz crystal.

TABLE 54 - UART BAUD RATES

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note[2]: The High Speed bit is located in the Device Configuration Space.
Using 1.8462 MHz Clock for <=38.4;
Using 1.843 MHz Clock for 115.2k;
Using 3.6864 MHz Clock for 230.4k;
Using 7.3728 MHz Clock for 460.8k

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
D. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:

- At least one character is in the FIFO
- The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay.)
- The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.
B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).
C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"),

XMIT interrupts occur as follows:
A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO POLLED MODE OPERATION

With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:
Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
Bit 5 indicates when the XMIT FIFO is empty.
Bit 6 indicates that both the XMIT FIFO and shift register are empty.
Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

EFFECT OF THE RESET ON REGISTER FILE

The Reset Function Table (**TABLE 55**) details the effect of $V_{cc}2$ POR or nRESET_OUT on each of the registers of the Serial Port.

TABLE 55 - RESET FUNCTION TABLE

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

TABLE 56 - REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

TABLE 56 - REGISTER SUMMARY FOR AN INDIVIDUAL UART CHANNEL (CONTINUED)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

UART REGISTER SUMMARY NOTES:

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.
Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

NOTES ON SERIAL PORT FIFO MODE OPERATION

GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. The UART will prevent loads to the Tx FIFO if it currently holds 16 characters. Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. To prevent the software from having to check for this situation the chip incorporates a timeout interrupt. The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it. These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

INFRARED COMMUNICATIONS CONTROLLER (IRCC 2.0)

The Infrared Communications Controller is fully compliant to the IrDA Specification Version 1.1 which includes data rates up to 4 Mbps to support IrDA-SIRA, IrDA-SIRB, IrDA-HDLC and IrDA-FIR modes. In addition the IRCC 2.0 provides support for ASK-IR, Consumer (TV remote) IR, and RAW-IR (Host controller has direct access to the IR bit stream from/to the transceiver module). It is important to note that the IRCC 2.0 block is a superset of a 16C550A UART. The IRCC 2.0 includes an Asynchronous Communications Engine (ACE) and a separate Synchronous Communications Engine (SCE) to provide the full set of IR modes as well as the standard UART Com mode. The IRCC 2.0 block details are fully described in SMSC's specification titled "Infrared Communications Controller". The information in this section of the specification will provide details on the integration of the FIR logic block into the FDC37N972 .

The infrared interface provides a two-way wireless communications port using infrared as a transmission medium. The IR transmission can use the standard IRTX and IRRX pins or optional IRTX2 and IRRX2 pins. These can be selected through the configuration registers. The IRTX2 and IRRX2 pins are alternate function pins.

IrDA-SIR allows serial communication at baud rates up to 115K Baud. Each word is sent serially beginning with a "0" value start bit. A "0" is signaled by sending a single IR pulse at the beginning of the serial bit time. A "1" is signaled by sending no IR pulse during the bit time. Please refer to the AC timing for the parameters of these pulses and the IrDA waveform. The Amplitude Shift Keyed IR allows serial communication at baud rates up to 19.2K Baud. Each word is sent serially beginning with a "0" value start bit. A "0" is signaled by sending a 500 kHz waveform for the duration of the serial bit time. A "1" is signaled by sending no transmission the bit time. Please refer to the AC timing for the parameters of the ASK-IR waveform.

If the Half Duplex option is chosen, there is a time-out when the direction of the transmission is changed. This time-out starts at the last bit transferred during a transmission and blocks the receiver input until the time-out expires. If the transmit buffer is loaded with more data before the time-out expires, the timer is restarted after the new byte is transmitted. If data is loaded into the transmit buffer while a character is being received, the transmission will not start until the time-out expires after the last receive bit has been received. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The time-out is four character times. A character time is defined as 10 bit times regardless of the actual word length being used.

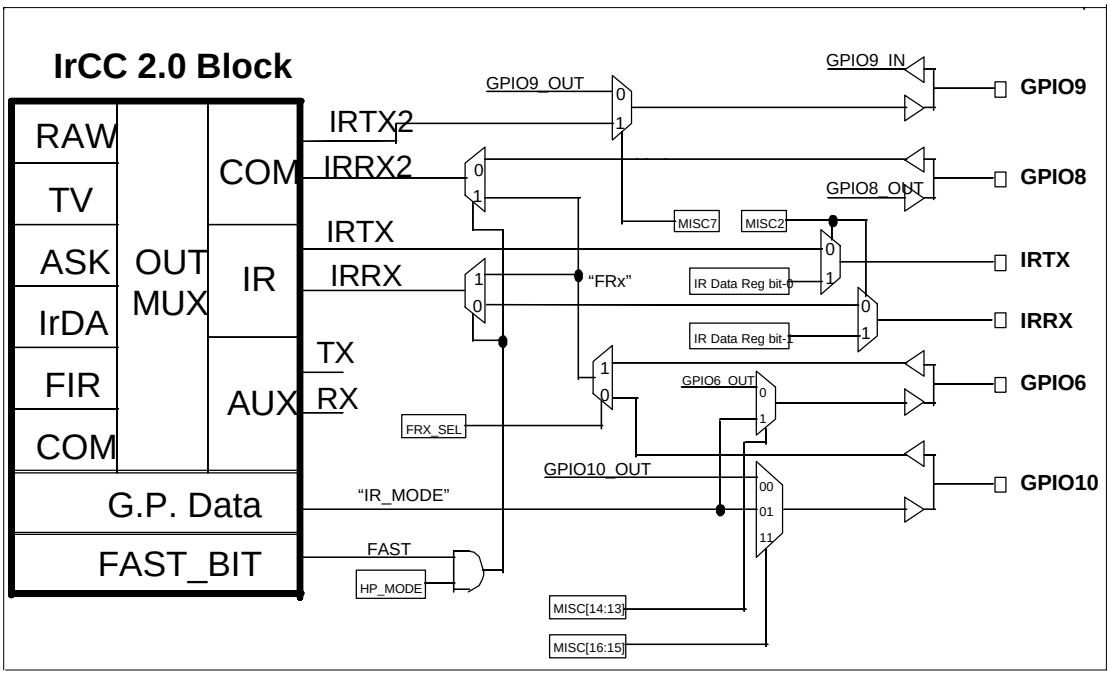


FIGURE 9 - INTEGRATION OF IRCC 2.0 LOGIC INTO THE FDC37N972

HP_MODE = (MISC[14:13] == [1:0]) | (MISC[16:15] == [1:0])
FRX_SEL = (MISC[14:13] == [1:0])

OVERVIEW

1. The FDC37N972 requires additional configuration register support to accommodate the IrCC 2.0 core.
2. NOTE: The IrCC 2.0 is configured in Logical Device Number 5. LD5 is still technically considered the Serial Port 2 block, even though UART2 is not included in the FDC37N97.

IRRX/IRTX PIN ENABLE

When MISC2=0 the IRRX and IRTX pins are enabled as when IrCC 2.0 (LD5) is activated or enabled and the IRCC 2.0 Output Mux is set to use the IR Port, otherwise the IRTX pin is tri-stated. When MISC2=1, the IRRX and IRTX pins are always enabled as they can be bit banged through the IR Data Register, bits 1 and 0 respectively.

Therefore, if the IR interface is on IRRX (pin 21) and IRTX (pin 20), then MISC2 allows the IR interface to be switched between the IRCC 2.0 block and the IR Data Register. The IR Data Register is only available from the host, and is located at index register 98. This register is available through the Mailbox Register Interface.

IR REGISTERS - LOGICAL DEVICE 5

CONFIGURATION REGISTERS OVERVIEW

In order to support the Infrared Communications Controller ten configuration registers are included in Logical Device 5. Refer to the Configuration section of this specification for details.

BASE I/O ADDRESSES

550 UART

TABLE 57 - ASYNCHRONOUS COMMUNICATIONS ENGINE (UART) REGISTER

REGISTER INDEX	BASE I/O RANGE	FIXED REGISTER BASE OFFSETS
0x60, 0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB | LSB div +1 : IER | MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR

Register 0x60 stores the MSB and 0x61 the LSB of the 550-UART's 16 bit Base Address.

FAST IR/SCE

TABLE 58 - SYNCHRONOUS COMMUNICATIONS ENGINE (SCE) REGISTERS

REGISTER INDEX	BASE I/O RANGE	FIXED REGISTER BASE OFFSETS
0x62, 0x63	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Register Block, address 0 +1 : Register Block, address 1 +2 : Register Block, address 2 +3 : Register Block, address 3 +4 : Register Block, address 4 +5 : Register Block, address 5 +6 : Register Block, address 6 +7 : SCE Master Control Register

Register 0x60 stores the MSB and 0x61 the LSB of the 550-UART's 16 bit Base Address.
Note: Refer to the Infrared Communications Controller (IRCC 2.0) Specification for register details.
Note: If Base I/O Address is set below 0x100 then no decode will occur.

IR DMA CHANNELS

DMA channel 0, 1, 2 or 3 may be selected for use with the IRCC 2.0 logic through the configuration registers of Logical Device 5. Refer to the Configuration section of this specification for further details on setting the DMA channel and to the IRCC 2.0 specification for details on IR DMA transfers.

IR IRQs

The interrupt (IRQ) for the IRCC 2.0 logic is selectable through the configuration registers for logical device 5. Refer to the Configuration section of this specification for further details on setting the IRQ and to the IRCC 2.0 specification for details on IR IRQ events.

Software Select Registers A and B

The Software Select A and Software Select B registers in the FDC37N972 configuration space in Logical Device Number 5 are directly connected to the read-only IrCC 2.0 Software Select A & B registers in SCE Register Block Three.

The FDC37N972 Software Select A register is LD5:CRF7, the FDC37N972 Software Select B register is LD5:CRF8. These registers are R/W.

Writing to LD5:CRF7 is the only way to revise the contents of the Software Select A register in the IrCC 2.0. Writing the contents of the Software Select A register can only be done in the configuration state and only after the LDN has been set to "5" and the CSR has been initialized to "F7H". The default value of this register after power up is 00H (**TABLE 59**).

Writing to LD5:CRF8 is the only way to revise the contents of the Software Select B register in the IrCC 2.0. Writing the contents of the Software Select B register can only be done in the configuration state and only after the LDN has been set to "5" and the CSR has been initialized to "F8H". The default value of this register after power up is 00H (**TABLE 59**).

TABLE 59 - FDC37N972 SOFTWARE SELECT A&B REGISTERS

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
LD5:CRF7	R/W	Software Select A								0x00
LD5:CRF8	R/W	Software Select B								0x00

IR HALF DUPLEX TIMEOUT

LD5:CRF2 is the FDC37N972 IR Half Duplex Time-Out register (**TABLE 60**). In the FDC37N972, this register is linked to the IrCC 2.0 IR Half Duplex Time-Out register.

In the FDC37N972, these two registers must behave like the other IrCC 2.0 legacy controls where either source uniformly updates the value of both registers registers when either register is explicitly written using IOW or following a device-level POR. IrCC 2.0 software resets do not affect these registers.

The IR Half Duplex Time-Out constrains the timing of transmit/receive direction mode changes in the IrCC 2.0. The IR Half Duplex Time-Out is started as each IR message data bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data is transferred in the current direction mode.

The IR Half Duplex Time-Out is programmable from 0 to 25.5ms in 100µs increments, as follows:

IR HALF DUPLEX TIME-OUT = (CRF2) x 100µs

TABLE 60 - IR HALF DUPLEX TIME-OUT REGISTER

		D7	D6	D5	D4	D3	D2	D1	D0	Default
LD5:CRF2	R/W	IR HALF DUPLEX TIME-OUT								0x03

IRTX OUTPUT PINS DEFAULT

The IRCC 2.0 IRTX pins default at power-up to “output”, “low” to prevent infrared transceiver damage. This default behavior applies to both the dedicated IRTX2 pin and to GPIO9 (see General Purpose I/O (GPIO) on page 265).

PARALLEL PORT

The FDC37N972 incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up. The functionality of the parallel port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below:

TABLE 61 - ADDRESS MAP FOR PARALLEL PORT

REGISTER NAME	ADDRESS
DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H
EPP ADDR PORT	BASE ADDRESS + 03H
EPP DATA PORT 0	BASE ADDRESS + 04H
EPP DATA PORT 1	BASE ADDRESS + 05H
EPP DATA PORT 2	BASE ADDRESS + 06H
EPP DATA PORT 3	BASE ADDRESS + 07H

TABLE 62 - THE BIT MAP OF THESE REGISTERS IS:

	D0	D1	D2	D3	D4	D5	D6	D7	NOTE
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	1
CONTROL PORT	STROBE	ALF	nINIT	SLC	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	AD7	2,3
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2,3

Note 1: These registers are available in all modes.
Note 2: These registers are only available in EPP mode.
Note 3 : For EPP mode, IOCHRDY must be connected to the ISA bus.

TABLE 63 - PARALLEL PORT CONNECTOR PIN MAP

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	129	nSTROBE	nWrite	nSTROBE
2-9	124-121, 119-116	PData<0:7>	PData<0:7>	PData<0:7>
10	115	nAck	Intr	nAck
11	114	Busy	nWait	Busy, PeriphAck(3)
12	113	PE	(NU)	PError, nAckReverse(3)
13	112	Select	(NU)	Select
14	128	Nalf	nDatastb	nALF, HostAck(3)
15	127	NError	(NU)	nFault(1) nPeriphRequest(3)
16	126	NInit	(NU)	nInit(1) nReverseRqst(3)
17	125	NSelectin	nAddrstrb	nSelectIn(1,3)

(1)= Compatible Mode (3)= High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE P1284 D2.0 Standard, "Standard Signaling Method for a Bi-directional Parallel Peripheral Interface for Personal Computers", September 10, 1993. This document is available from the IEEE.

IBM XT/AT COMPATIBLE, BI-DIRECTIONAL AND EPP MODES

DATA PORT
ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0-PD7 ports. During a READ operation in SPP mode, PD0-PD7 ports are buffered (not latched) and output to the host CPU.

STATUS PORT
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an nIOR read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 μsec time out has occured on the EPP bus. A logic "0" means that no time out error has occured; a logic "1" means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a "0". Writing a "0" to this bit has no effect.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR
The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic “1” means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic “1” means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic “1” indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 nACK - nACKNOWLEDGE
The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic “0” means that the printer has received a character and can now accept another. A logic “1” means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic “0” in this bit means that the printer is busy and cannot accept a new character. A logic “1” means that it is ready to accept the next character.

CONTROL PORT
ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 ALF - AUTOFEED
This bit is inverted and output onto the nALF output. A logic “1” causes the printer to generate a line feed after each line is printed. A logic “0” means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the nSLCTIN output. A logic “1” on this bit selects the printer; a logic “0” means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic “1” means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written

EPP ADDRESS PORT
ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP ADDRESS WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0-PD7 ports are read, the leading edge of IOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 0
ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0-PD7 ports, the leading edge of nIOW causes an EPP DATA WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

EPP DATA PORT 1
ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 2
ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP DATA PORT 3
ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 OPERATION

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, ALF, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10µsec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e. a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. IOCHRDY is driven active low at the start of each EPP write and is released when it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1.If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
2.If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host selects an EPP register, places data on the SData bus and drives nIOW active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
5. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
6. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
7. a)The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b)The chip latches the data from the SData bus for the PData bus and asserts (releases) IOCHRDY allowing the host to complete the write cycle.
8. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
9. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

EPP 1.9 READ

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. IOCHRDY is driven active low at the start of each EPP read and is released when it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1.If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.

2.If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host selects an EPP register and drives nIOR active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip tri-states the PData bus and deasserts nWRITE.
5. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
6. Peripheral drives PData bus valid.
7. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
8. a)The chip latches the data from the PData bus for the SData bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.
   b)The chip drives the valid data onto the SData bus and asserts (releases) IOCHRDY allowing the host to complete the read cycle.
9. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
10. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.

EPP 1.7 OPERATION

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, ALF, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10µsec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to the end of the cycle nIOR or nIOW deasserted). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for and EPP read.

EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

The host sets PDIR bit in the control register to a logic "0". This asserts nWRITE.
The host selects an EPP register, places data on the SData bus and drives nIOW active.
The chip places address or data on PData bus.
Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.

When the host deasserts nIOW the chip deasserts nDATASTB or nADDRSTRB and latches the data from the SData bus for the PData bus.

Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

EPP 1.7 READ

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.
2. The host selects an EPP register and drives nIOR active.
3. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4. If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. When the host deasserts nIOR the chip deasserts nDATASTB or nADDRSTRB.
8. Peripheral tri-states the PData bus.
9. Chip may modify nWRITE, PDIR and nPDATA reparation of the next cycle.

TABLE 64 - EPP PIN DESCRIPTIONS

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output/write condition and a high means an input/read condition. This signal is normally a low (output/write) unless PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.
Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

EXTENDED CAPABILITIES PARALLEL PORT

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel
Interlocked handshake, for fast reliable transfer
Optional single byte RLE compression for improved throughput (64:1)
Channel addressing for low-cost peripherals
Maintains link and data layer separation
Permits the use of active output drivers
Permits the use of adaptive signal timing
Peer-to-peer capability

VOCABULARY

The following terms are used in this document:

assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward: Host to Peripheral communication.
reverse: Peripheral to Host communication.

PWord: A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.
1: A high level.
0: A low level.

These terms may be considered synonymous:

PeriphClk, nAck
HostAck, nALF
PeriphAck, Busy
nPeriphRequest, nFault
nReverseRequest, nInit

nAckReverse, PError
Xflag, Select
ECPMode, nSelectIn
HostClk, nSTROBE

Reference Document

IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.14, July 14, 1993. This document is available from Microsoft.

TABLE 65 - BIT MAP OF THE EXTENDED PARALLEL PORT REGISTERS

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	alf	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	0	0	0	0	0	0	
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.

ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

DESCRIPTION

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

TABLE 66 - ECP PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
nSTROBE	O	During write operations nSTROBE registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nALF in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nSTROBE in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nSTROBE. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.

NAME	TYPE	DESCRIPTION
nALF (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

REGISTER DEFINITIONS

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other that those specified is undefined.

TABLE 67 - ECP REGISTER DEFINITIONS

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

TABLE 68 - EXTENDED CONTROL REGISTER MODE DESCRIPTIONS

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mde
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

*Refer to ECR Register Description

DATA AND ECPAFIFO PORT
ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmitts this byte to the peripheral automatically. The operation of this register is ony defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet .

DEVICE STATUS REGISTER (DSR)
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0-2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault
The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck
The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 nBusy
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

DEVICE CONTROL REGISTER (DCR)
ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 ALF - AUTOFEED
This bit is inverted and output onto the nALF output. A logic “1” causes the printer to generate a line feed after each line is printed. A logic “0” means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the nSLCTIN output. A logic “1” on this bit selects the printer; a logic “0” means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

BIT 5 DIRECTION
If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic “1” means that the printer port is in input mode (read).

BITS 6 and 7 during a read are a low level, and cannot be written.

CFIFO (PARALLEL PORT DATA FIFO)
ADDRESS OFFSET = 400H

Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ECPDFIFO (ECP DATA FIFO)
ADDRESS OFFSET = 400H

Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is "0", are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is "1". Reads or DMAs from the FIFO will return bytes of ECP data to the system.

TFIFO (TEST FIFO MODE)
ADDRESS OFFSET = 400H

Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics. The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be derermined by starting with a full tFIFO, setting the direction bit to "0" and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be derermined by setting the direction bit to "1" and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

CNFGA (CONFIGURATION REGISTER A)
ADDRESS OFFSET = 400H

Mode = 111

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)
ADDRESS OFFSET = 401H

Mode = 111

BIT 7 compress
This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

BIT 6 intrvalue
Returns the value on the ISA iRq line to determine possible conflicts.

BITS 5:0 Reserved
During a read are a low level. These bits cannot be written.

ecr (Extended Control Register)
ADDRESS OFFSET = 402H
Mode = all
This register controls the extended ECP parallel port functions.

BITS 7 - 5
These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.
case dmaEn=1:
During DMA (this bit is set to a “1” when terminal count is reached).
case dmaEn=0 direction=0:

This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.
case dmaEn=0 direction=1:
This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full
Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

BIT 0 empty
Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

TABLE 69 - EXTENDED CONTROL REGISTER

R/W	MODE
000:	Standard Parallel Port Mode . In this mode the FIFO is reset and common collector drivers are used on the control lines (nSTROBE, nALF, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register L3-CRF0. All drivers have active pull-ups (push-pull).
101:	Reserved
R/W	**MODE**
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

OPERATION

MODE SWITCHING/SOFTWARE CONTROL

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ecp reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ecp reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nALF independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

ECP OPERATION

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

Set Direction = 0, enabling the drivers.
Set strobe = 0, causing the nSTROBE signal to default to the deasserted state.
Set alf= 0, causing the nALF signal to default to the deasserted state.
Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to “1” or “0”, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

TERMINATION FROM ECP MODE

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

COMMAND/DATA

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8 bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low. The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always "0". Reverse channel addresses are seldom used and may not be supported in hardware.

TABLE 70 - FORWARD CHANNEL COMMANDS (HOSTACK LOW) & REVERSE CHANNEL COMMANDS (PERIPACK LOW)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

DATA COMPRESSION

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

PIN DEFINITION

The drivers for nSTROBE, nALF, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

ISA CONNECTIONS

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section.) Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

INTERRUPTS

The interrupts are enabled by serviceIntr in the ecr register.
serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.
An interrupt is generated when:
1. For DMA transfers: When serviceIntr is “0”, dmaEn is 1 and the DMA TC is received.
2. For Programmed I/O:
a. When serviceIntr is 0, dmaEn is 0, direction is “0” and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
b. (1) When serviceIntr is “0”, dmaEn is 0, direction is “1” and there are readIntrThreshold or more bytes in the FIFO. (2) An interrupt is also generated when serviceIntr is cleared to “0” whenever there are readIntrThreshold or more bytes in the FIFO.
3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from “1” to “0” and nFault is asserted.
4. When ackIntEn is “1” and the nAck signal transitions from a low to a high.

FIFO OPERATION

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA TRANSFERS

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to “1” and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting nPDACK and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until nPDACK is deasserted for

a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers is with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to “0”, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to “1”, followed by setting serviceIntr to 0.

DMA MODE - TRANSFERS FROM THE FIFO TO THE HOST

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by nPDACK), indicating that no more data is required. PDRQ goes inactive after nPDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nPDACK). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and serviceIntr has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle).

PROGRAMMED I/O MODE OR NON-DMA MODE

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0. The ECP requests programmed I/O transfers from the host by activating the PINTR pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

PROGRAMMED I/O - TRANSFERS FROM THE FIFO TO THE HOST

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold = (16-<threshold>) data bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can

be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

PROGRAMMED I/O - TRANSFERS FROM THE HOST TO THE FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into theFIFO.

PARALLEL PORT INTERFACE MULTIPLEXOR

THE PARALLEL PORT PHYSICAL INTERFACE (PPPI)

The Parallel Port Physical Interface (PPPI) may be owned and controlled by any of threesources. The sources are detailed as follows:

TABLE 71 - PARALLEL PORT MULTIPLEXING OPTIONS

PPPI CONTROLLING SOURCE DEVICE	DESCRIPTION	CONFIG REGISTER 0X25 BITS[4:3]	PP_HA
8051	The parallel port physical interface is configured as a SPP mode bi-directional parallel port controlled directly by the 8051 through a set of memory mapped external RAM registers.	[X:X]	0
FDC	The parallel port physical interface is configured as a standard Floppy Disk Drive interface. All configuration and control bits pertaining to the FDC logical device apply to the PPPI in this mode	[1:0] or [0:1]	1
Host	The parallel port physical interface is configured as the legacy parallel port which supports Compatible, SPP, EPP and ECP modes of operation. All configuration and control bits pertaining to the parallel port logical device apply to the PPPI in this mode.	[0:0] or [1:1]	1

When the Host (Parallel Port logical device) owns/controls the parallel port interface, its state (i.e., pwrdown) determines the states of the pins. When the FDC (FDC logical device) owns/controls the Parallel Port interface, its state (i.e., powerdown) determines the state of the pins. When the 8051 controls/owns the parallel port interface, it has direct control of the Parallel Port Physical Interface pins. Under 8051 control the Parallel Port Output pins are always enabled or driven and only tri-state when VCC2 is removed (powergood=0).

If the Host does not have control of the Parallel Port Physical Interface (PPPI), then it is left as a function of the software driver or BIOS to de-activate the DRQ and IRQ of the Parallel Port Logical Device by either setting its DMA Channel Select Configuration Register to 0x04 and its Interrupt Select Configuration Regsiter to 0x00 or by clearing the Parallel Port Logical Device's Activate bit. Also, if the Host does not have control of the PPPI, then the following parallel port logical device registers are read as follows.

Data Register (read) = last Data Register (write).

Control Register (read): read as "cable not connected" [STROBE, LF, and SLC = 0 and nINIT = 1.

Status Register (read): nBUSY, PE, SLCT = 0, nACK, nERR = 1.

Note: Bit D7 of the 8051 memory mapped DISABLE register (parallel port enable bit) has no effect on the parallel port physical interface pins when the port is owned by any source other than the the Host (parallel port logical device).

HOST (LEGACY) PARALLEL PORT INTERFACE (FDC37N972 STANDARD)

In this mode, the parallel port pins are controlled by the host through the parallel port logical device. Refer to the Configuration section and the Parallel Port section for information on the configuration and control registers respectively.

PARALLEL PORT FDC INTERFACE

In this mode, the floppy disk control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available to the Host.

PARALLEL PORT FDC PIN OUT

The FDC signals are muxed onto the 'Parallel Port pins as shown in the following table. Outputs are OD14, Open Drain which sink 14ma.

TABLE 72 - PARALLEL PORT FLOPPY PIN OUT

	PARALLEL PORT SPP MODE		FDC MODE	
CONNECTOR PIN #	SIGNAL NAME	PIN DIRECTION	SIGNAL NAME	PIN DIRECTION
1	nSTROBE	I/O	nDS0	(O)*
2	PD0	I/O	nINDEX	I
3	PD1	I/O	nTRK0	I
4	PD2	I/O	nWP	I
5	PD3	I/O	nRDATA	I
6	PD4	I/O	nDSKCHG	I
7	PD5	I/O	-	-
8	PD6	I/O	nMTR0	(O)*
9	PD7	I/O	-	-
10	NACK	I	nDS1	(O)*
11	BUSY	I	nMTR1	(O)*
12	PE	I	nWDATA	O
13	SLCT	I	nWGATE	O
14	nALF	I/O	DRVDEN0	O
15	nERR	I	nHDSEL	O
16	nINIT	I/O	nDIR	O
17	nSLCTIN	I/O	nSTEP	O

*These pins are outputs in mode PPFD2; in mode PPFD1 only one pair, depending on Drive Swap bit, is active and should be connected to the FDD, the inactive pair should not be connected to the FDD.

PARALLEL PORT FDC CONTROL

There are two modes of operation, PPFD1 and PPFD2. These modes can be selected in Global Configuration Register 0x25 (Device Mode), bits 3 and 4. PPFD1 mode has only drive 1 on the parallel port pins; PPFD2 mode has drive 0 and 1 on the parallel port pins. Note: The Drive Swap bit, FDD Mode Configuration Register bit-4 (LD0_CRF0), can be used to swap the motor and drive select outputs on of the Parallel Port FDC.

TABLE 73 - PARALLEL PORT FDC MODES OF OPERATION

PPFD1:	Drive 0 is on the FDC pins. Drive 1 is on the parallel port pins.	Drive Swap bit = 0
	Drive 1 is on the FDC pins. Drive 0 is on the parallel port pins.	Drive Swap bit = 1
PPFD2:	Drive 0 is on the parallel port pins. Drive 1 is on the parallel port pins.	

The following FDC output pins are Open Drain 14mA outputs when the Parallel Port FDC is selected by the drive select register. Reminder, it is up to the designer to provide pull-up resistors on these FDC output pins.

nWDATA, DRVDEN0, nHDSELm nWGATE, nDIR, nSTEP, nDS1, nDS0, nMTR0, nMTR1.

PARALLEL PORT - 8051 CONTROL

In this mode, the parallel port pins are controlled by the 8051 through a set of three on-chip memory mapped registers. The memory mapped registers are the PAR PORT STATUS, the PAR PORT CONTROL, and the PAR PORT DATA registers. In this mode, the parallel port pins are not controlled by the parallel port logical device. Refer to the 8051 section of this specification for information on these control registers.

TABLE 74 - FDC ON PARALLEL PORT ACTIVATION CONTROL

FDC Parallel Port Mode CR25 Bits [4:3]	FDC Active Bit L0-CR30-Bit0	FDC in Power Down	Parallel Port Active Bit	Parallel Port In Power Down	PP_ HA	Parallel Port Pins (Mode) State
01 or 10	0	x	x	x	1	(FDC) Inactive
01 or 10	1	N	x	x	1	(FDC) Active
01 or 10	1	Y	x	x	1	(FDC) Inactive
00 or 11	X	x	0	x	1	(Parallel Port) Inactive
00	X	x	1	N	1	(Parallel Port) Active
00	X	x	1	Y	1	(Parallel Port) Inactive
00	X	x	x	x	0	(8051 Mode) Active

INACTIVE = HI-Z ON PINS
Active = OD14/O14 as per selected mode.
The FDD pins that are multiplexed onto the Parallel Port function independently of the state of the Parallel Port logical device. This affects the pins when CR25 bits [4:3] are 01 or 10.
(Note: FDC Mode Bits L0-CRF0-B[7:6] have no effect on the parallel port Pins).

AUTO POWER MANAGEMENT

Auto Power Management (APM) capabilities are provided for the following logical devices: Floppy Disk, UART, Infrared and the Parallel Port. For each logical device, two types of power management are provided; direct powerdown and auto powerdown.

SYSTEM POWER MANAGEMENT

See the “8051 System Power Management” section for details.

FDC POWER MANAGEMENT

Direct power management is controlled through Global Configuration Register 22 (CR22). Refer to CR22 in the Configuration section for more information.

Auto Power Management is enabled through bit-0 of CR23. When set, this bit allows the FDC to enter powerdown when all of the following conditions have been met:

1.The motor enable pins of the FDC’s DOR register are inactive (zero).
2.The FDC37N972 must be idle; the MSR register = 80h and the FDC’s INTerrupt = 0 (INT may be high even if MSR = 80H due to polling interrupts).
3.The head unload timer must have expired.
4.The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The

FDC37N972 is then powered down when all the conditions are met.

Disabling the auto powerdown mode cancels the timer and holds the FDC block out of auto powerdown.

DSR FROM POWERDOWN

Bit 6 of the FDC's DSR register is another FDC powerdown bit. If DSR powerdown is used when the FDC37N972 is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the FDC37N972 is awakened from DSR powerdown, the auto powerdown will once again become effective.

WAKE UP FROM AUTO POWERDOWN

If the FDC37N972 enters the Powerdown State through the auto powerdown mode, then the FDC37N972 can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the FDC37N972 will go through the normal reset sequence. If the access is through the selected registers, then the FDC resumes operation as though it was never in powerdown. Besides activating the nRESET_OUT pin or one of the software reset bits in the DOR or DSR registers, the following register accesses will wake up the FDC37N972:

1. Seting any one of the motor enable bits in the DOR register (reading the DOR does not awaken the FDC37N972).
2. A read from the MSR register.
3. A read from or a write to the Data register.

Once awake, the FDC will reinitiate the auto powerdown timer for 10 ms. The FDC37N972 will powerdown again when all the powerdown conditions are satisfied.

REGISTER BEHAVIOR

TABLE 75 shows the AT and PS/2 (including Model 30) configuration registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers is maintained. As **TABLE 75** shows, two sets of registers are distinguished based on whether their access results in the FDC37N972 remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the FDC37N972. These registers can be accessed during powerdown without changing the status of the FDC37N972. A read from these registers will reflect the true status as shown in the register description in the FDC section. Writes to these registers will result in the FDC37N972 retaining the data and subsequently reflecting it when the FDC37N972 awakens. Accessing the FDC37N972 during powerdown may cause an increase in the power consumption by the FDC37N972. The FDC37N972 will revert back to its low power mode when the access has been completed.

PIN BEHAVIOR

The FDC37N972 is specifically designed for portable PC systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins which interface to the floppy disk drive are disabled so that no power will be drawn through the FDC37N972 as a result of any voltage applied to the pin within the VCC2 power supply range. Most of the pins that interface to the system are left active to monitor system accesses that may wake up the FDC37N972.

SYSTEM INTERFACE PINS

Table 76 gives the state of the system interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged". Input pins are "Disabled" to prevent them from causing currents internal to the FDC37N972 when they have indeterminate input values.

TABLE 75 - PC/AT AND PS/2 AVAILABLE REGISTERS

BASE + ADDRESS	AVAILABLE REGISTERS		ACCESS PERMITTED
	PC/AT	PS/2 (Model 30)	
Access to these registers DOES NOT wake up the FDC37N972			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR (1)	DOR (1)	R/W
03H	---	---	---
04H	DSR (1)	DSR (1)	W
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the FDC37N972			
04H	MSR	MSR	R
05H	Data	Data	R/W

Note 1: Writing to the DOR or DSR does not wake up the FDC37N972, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the FDC37N972.

TABLE 76 - STATE OF SYSTEM PINS IN FDC AUTO POWERDOWN

SYSTEM PINS	STATE IN AUTO POWERDOWN
Input Pins	
nIOR	Unchanged
nIOW	Unchanged
AEN	Unchanged
nMEMRD	Unchanged
nMEMWR	Unchanged
SA[15:0]	Unchanged
SD[7:0]	Unchanged
nNOWS	Unchanged(hi-Z)
nDACKx	Unchanged
TC	Unchanged
nROMCS	Unchanged
Output Pins	
nRESET_OUT	Unchanged
IRQx	Unchanged(low)
DB[0:7]	Unchanged
DRQx	Unchanged(low)
IOCHRDY	Unchange(n/a)

FDD INTERFACE PINS

All pins in the FDD interface, which can be connected directly to the floppy disk drive itself, are either DISABLED or TRISTATED. Pins used for local logic control or part programming are unaffected. Table 77 depicts the state of the floppy disk drive interface pins in the Powerdown State.

FDD POWER DOWN PIN (FPD) BEHAVIOR

The FPD pin can be used to automatically shut off power to the floppy disk drive when it is not required. The FPD pin is an active high output signal that is driven based on the states of the FDC. Whenever the FDC Shutdown bit is set (see FDD Mode Register, bit-5 in the Configuration Register Section) the FPD pin goes high. If the FDC Shutdown bit is not set then the FPD pin will go high whenever the FDC bit (see bit 0 of the Power Mgmt Register in the Configuration Section) is set and the FDC has entered an auto powerdown state as described above. If neither the FDC Shutdown bit nor the FDC bit are set then the FPD pin goes active "high" when the Power- down bit is set (see bit 6 of the Data Rate Select Register [DSR]) and "low" when the Powerdown bit is cleared. Refer to Table 78 - FDD POWER DOWN PIN BEHAVIOR.

TABLE 77 - STATE OF FLOPPY DISK DRIVE INTERFACE PINS IN FDC POWERDOWN

FDD PINS	STATE IN FDC AUTO POWERDOWN
Input Pins	
nRDATA	Input
nWPROT	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
Output Pins	
nMTR[1:0]	Tristated
nDS[1:0]	Tristated
nDIR	Active
nSTEP	Active
nWDATA	Tristated
WGATE	Tristated
nHDSEL	Active
DRVDEN[1:0]	Active
FPD	Active

Table 78 - FDD POWER DOWN PIN BEHAVIOR

POWER DOWN BIT, DSR, BIT-6	FDC BIT, GCR23 BIT-0 AUTO POWER DOWN	FDC SHUTDOWN BIT, FDD MODE REGISTER	FPD PIN STATE
0	0	0	0
POWER DOWN BIT, DSR, BIT-6	**FDC BIT, GCR23 BIT-0 AUTO POWER DOWN**	**FDC SHUTDOWN BIT, FDD MODE REGISTER**	**FPD PIN STATE**
1	0	0	1
X	1	0	1 (Note)
X	X	1	1

Note: The FPD pin will go active when the FDC auto powers down. Refer to the FDC auto power management section for more details.

UART POWER MANAGEMENT

Direct power management is controlled by CR22. Refer to CR22 in the Configuration Section for more information.

Auto power management is enabled by CR23 bit 4 and bit 5. When set, these bits allow the following auto power management operations:
1.The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2.The receiver enters powerdown when the following conditions are all met:
A. Receive FIFO is empty
B. The receiver is waiting for a start bit

Note: While in powerdown the Ring Indicator interrupt is still valid.

EXIT AUTO POWERDOWN

The transmitter exits powerdown on a write to the transmit buffer. The receiver exits auto powerdown when RXD changes state.

PARALLEL PORT POWER MANAGEMENT

Direct power management is controlled by CR22. Refer to CR22 in the Configuration Section for more information.

Auto power management is enabled by CR23 bit 3. When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into powerdown when not being used.

The EPP logic is in powerdown under any of the following conditions:
EPP is not enabled in the configuration registers.
EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

ECP is not enabled in the configuration registers.
SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

XIT AUTO POWERDOWN

The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

8051 EMBEDDED CONTROLLER

8051 FUNCTIONAL OVERVIEW

The High-Performance 8051 embedded controller is a fully static CMOS core compatible with the industry- standard 80C51 microcontroller. The high-performance 8051 features include:

2.5X average instruction execution speed improvement over the entire instruction set; i.e., typical 4-clock instruction cycle in high-performance 8051 vs. 12-clock instruction cycle in standard 8051.
Faster clock speed: 24MHz or higher vs. 16MHz in standard 8051.
Dual Data Pointers
More Interrupts: Power-Fail, External Interrupt 2, External Interrupt 3, etc.

A set of External Memory/Mapped Control Registers provides the 80C51 core with the ability to directly control many functional blocks of the FDC37N972.

This section concentrates on the FDC37N972 enhancements to the 80C51. For Non-Standard Special Function Registers, interrupt processing and Timer 2 functions see Appendix B. For general information about the 80C51, refer to the Hardware Description of the 8051, 8052, and_80C51 and the 80C51BH-1/80C51BH-2 CHMOS Single-Chip 8 Bit Microcomputer data sheets in the 8 Bit Embedded Controller Handbook.

FEATURES

16x32K External ROM
256 Byte Internal Scratch ROM
256 Bytes Internal RAM
256 Bytes of External RAM
256 Byte External Memory/Mapped Control Register Area
128 Byte Special Function Register Area
Access to 256 Byte RTC CMOS RAM
8042 style Keyboard Controller Host Interface
Eleven Interrupt Sources
Watch Dog Timer (WDT)
Ring Oscillator with Fail Safe Control

High-Performance 8051 Implemented Features

There are five significant features implemented in the high-performance 8051 core. These features, summarized in TABLE 79, are described more fully in the sub-sections that follow.

TABLE 79 - HIGH-PERFORMANCE 8051 IMPLEMENTED FEATURES

FEATURE	VALUE	DESCRIPTION
Internal RAM Size	256 (bytes)	The internal RAM size is 256 bytes to maintain compatibility with existing implementations.
Internal Timers (Note)	3	There are three internal Timers (T0, T1 & T2).
Internal ROM Size	2048 (bytes)	The internal ROM size is 2048 bytes to maintain compatibility with existing implementations.
Serial Ports	1	There is one Serial Port.
Interrupts	11	The high-performance 8051 interrupt unit provides 11 interrupt sources (see **TABLE 92**).

Note: The external inputs for Timer/Counter T0, T1, and T2, as well as the Timer/Counter 2 capture/reload trigger T2EX are not supported in the FDC37N972.

FUNCTIONAL BLOCKS

Below are the functional blocks that the 8051 core has control of through its on-chip memory/mapped external registers.

8042 Style Keyboard Controller Interface
Extended Interrupts
Power Management Functions
Direct Keyboard Scan Matrix (up to 128 keys)
Four channel PS/2 Interface
Dual Access Bus Interface
LED controls
Two Pulse Width Modulators
RTC CMOS RAM Access
8051 Control of the Parallel Port Interface
42 General Purpose I/O (GPIO) pins
ACPI Embedded Controller
PM1 Block

HIGH-PERFORMANCE 8051 CYCLE TIMING AND INSTRUCTION SET

The high-performance 8051 processor offers increased performance by executing instructions in a 4-clock cycle, as opposed to the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectutres.

Some instructions require a different number of instruction cycles on the high-performance 8051than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. In the high-performance 8051 architecture, instructions can take between one and five instructions to complete. The average speed improvement for the entire instruction set is approximately 2.5X. See TABLE 253 - 8051 INSTRUCTION SET on page 380 for number of cycles on individaul instruction requries.

POWERING UP OR RESETTING THE 8051

DEFAULT RESET CONDITIONS

The FDC37N972 has two sources of reset: a VCC1 Power On Reset (VCC1 POR) or a VCC2 POR. An FDC37N972 reset from any of these sources will cause the hardware response shown in TABLE 86, 8051 On-Chip External Memory Mapped Registers. Note that the values shown are those prior to any resident firmware control. Refer to TABLE 86 for the effect of each type of reset on each of the on-chip registers.

POWER-UP SEQUENCE

When the 8051 first powers up by VCC1, the ring oscillator is started, once this has stabilized, the 8051 starts executing from program address 00. Once running, the 8051 can access all of the registers that are on VCC1 and if VCC2 is at 3.3V it can access all of the registers on VCC2. For on-chip registers powered by VCC1 which are reset upon VCC2 Power On Reset (VCC2 POR), it is important that 8051 firmware not initialize or write to any of these registers until 1ms following VCC2 = 3.3V AND PWRGD = 1 (See TABLE 86.)

Note: In order to guarantee that the external Flash device has powered up and is ready to operate before the 8051 attempts to access it, the internal VCC1 POR pulse has been extended to 20ms. The internal VCC1 POR signal is asserted upon VCC1 reaching a valid level and will remain asserted for a period of 20ms following the assertion of the VCC1_PWRGD pin.

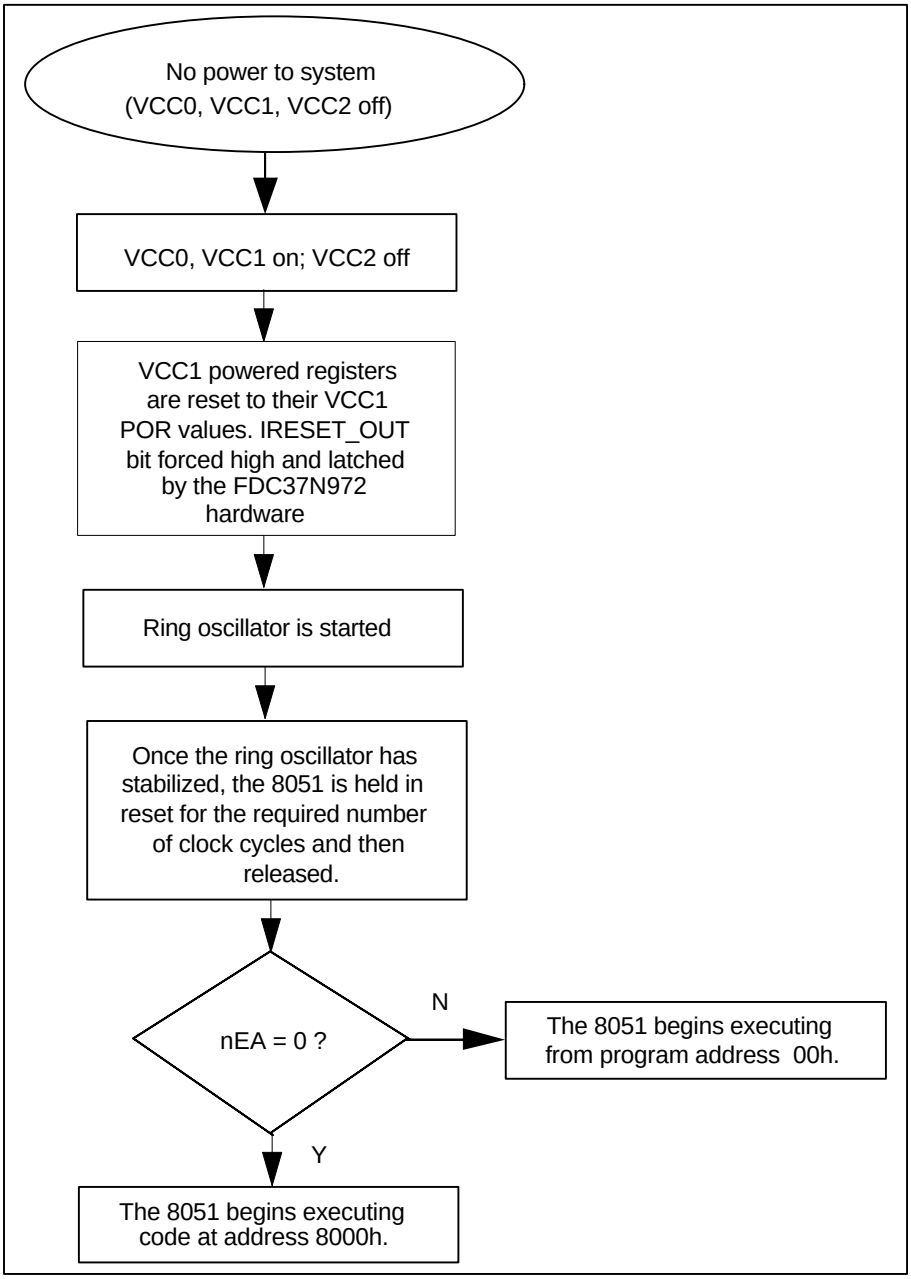


FIGURE 10 - SYSTEM POWER UP SEQUENCE

SYSTEM RESET SEQUENCE

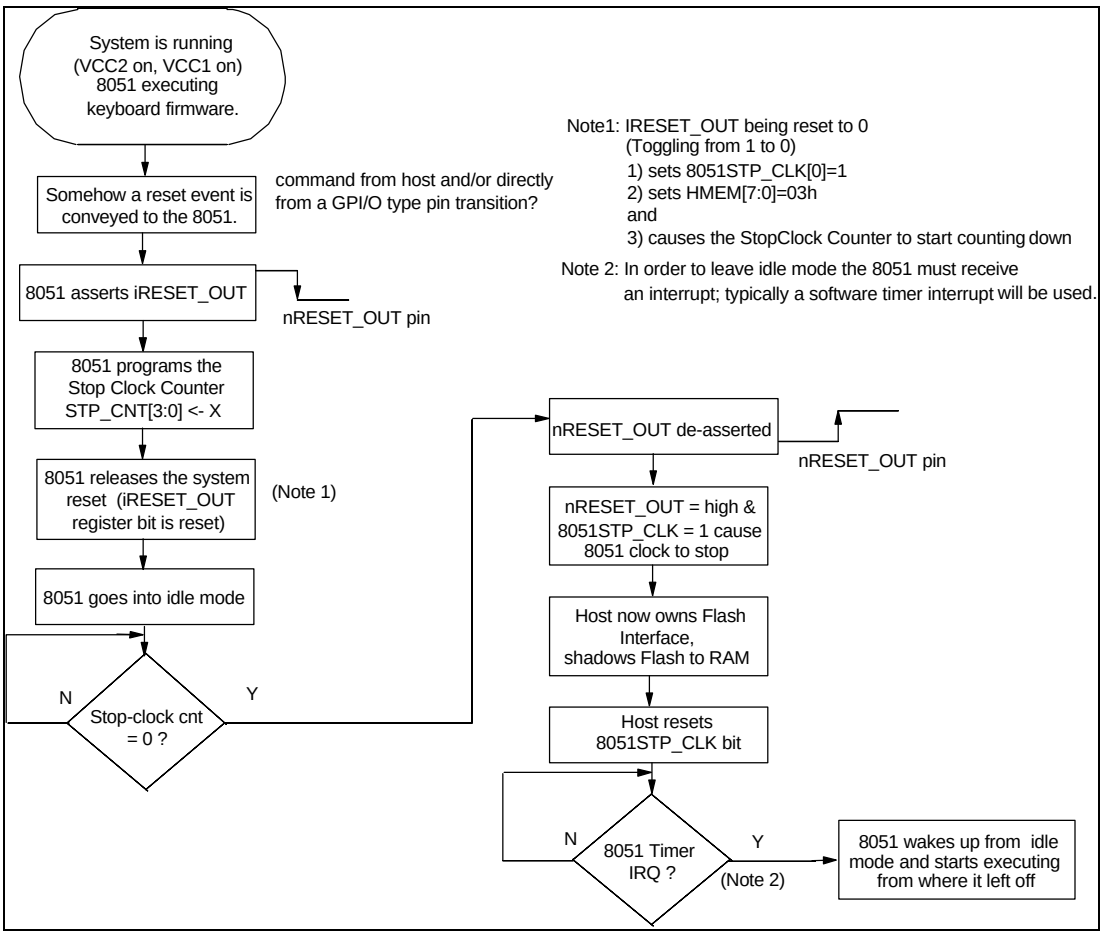


FIGURE 11 - TYPICAL SYSTEM RESET SEQUENCE

CPU RESET SEQUENCE

Often the Host CPU (x486 or Pentium) is reset by the hardware signal, CPU_RESET, which is issued by software to switch the Processor from Protected, or "Virtual 86", mode back to Real mode. CPU_RESET can be generated from the FDC37N972 8051 core or it may be generated from other logic on the PC motherboard. CPU_RESET is meant only to reset the CPU; the rest of the system continues to run normally, including the keyboard BIOS in the 8051.

Reacting to the CPU_RESET, the CPU performs a code fetch to a reset vector address that is located 16 bytes below the top address of memory (4GB - 16B). This generates an active nROMCS to the FDC37N972 along with memory RD strobes, but since the 8051 has not passed control of the Flash interface to the Host CPU the FDC37N972 must supply a set of emulated CPU instructions that cause the CPU to jump to its shadowed Boot vector address at (1MB - 16B).

If the host does not have control of the Flash when nROMCS and nMEMRD are simultaneously asserted, the FDC37N972 decodes the lower three System Address bits, SA[2:0] and presents the Host with 0xEA on the System Data Bus SD[7:0] when SA[2:0] = 0, or 0xF0 otherwise (FIGURE 12). This results in an opcode that instructs the Host CPU to perform an absolute jump to address 0xFFFF0, where the BIOS is shadowed.

NOTE: The FDC37N972 CPU reset sequence described above is independent of the Bonding Option.

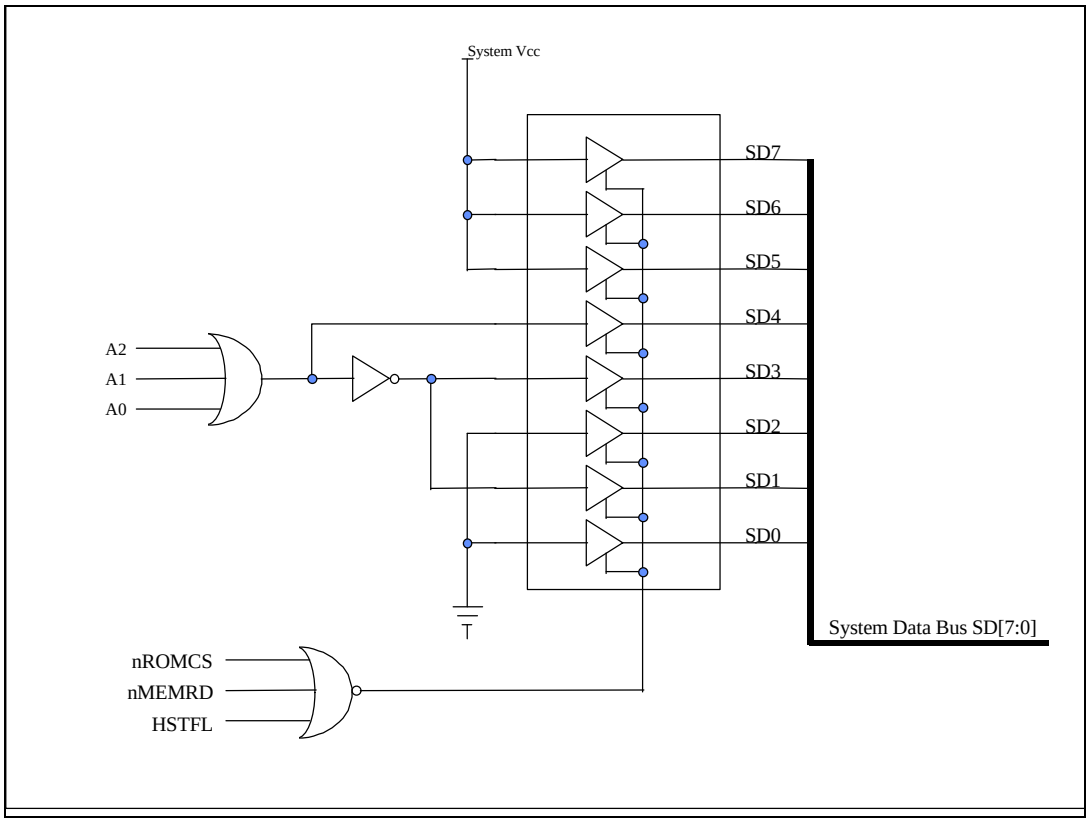


FIGURE 12 - SYSTEM RESET BOOT VECTOR

8051 CLOCK CONTROLS

CLOCK SOURCES

EXTERNAL CLOCK SIGNAL

The external clock source is from a 14.318MHz TTL compatible clock. VCC2 must be powered in order for this to occur.

INTERNAL CLOCK SIGNAL

The 8051 may program it self to run off of an internal ring oscillator having a frequency range between 4 and 12MHz. This is not a precise clock, but is meant to provide the 8051 with a clock source when VCC2 is shut down in the system.

Frequency Controls

The 8051 system clock frequencies are selected by the KBDCLK[1:0] control bits in the KSTP_CLK register. The KSTP_CLK register is MMCR 0x7F27.

In the KSTP_CLK register, the STP_CNT[3:0] bits are moved from the KSTP_CLK register to the STOP_COUNT register, the KBDCLK ENABLE bit and a RESERVED bit (possibly to control the 14.318 MHz PLL Power-Down function) are added to the KSTP_CLK register.

To “stop” the 8051 clock, use the KBDCLK ENABLE bit D0 in the KSTP_CLK register (TABLE 81).

TABLE 80 - STOP_COUNT REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F2F	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	RESERVED				STP_CNT[3:0]			

STP_CNT[X]

This defines the number of machine cycles from when the internal IRESET_OUT bit is cleared until the external nRESET_OUT pin goes inactive high (deasserts). The STP_CNT[3:0] bits are D0 – D3 in the FDC37N972 KSTP_CLK Register.

TABLE 81 - KSTP_CLK REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F27	VCC1	0x10

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R	R	R/W	R/W
BIT NAME	KBDCLK[1:0][1]		KBCLK/ROSC	ROSCEN	RESERVED		PLL_STOP	KBDCLK ENABLE

KBDCLK/ENABLE

When the KBDCLK ENABLE bit is “0”, the 8051 PLL clock is stopped, like when the KBDCLK[1:0] = 0,0 in the FDC37C95X. When KBDCLK ENABLE is “1”, the 8051 PLL clock is running.

PLL_STOP

The PLL_STOP bit D1 is used to control the power state of the 14.318MHz PLL. When the PLL_STOP bit is “1” the PLL and all of the internal clocks except for the RTC and Ring Oscillator are stopped. When the PLL_STOP bit is “0” the PLL and all of the internal clocks are running. When VCC2 is active and the PLL_STOP bit changes from “1” to “0”, there is a delay of 100µs max. before the PLL clocks are stable.

ROSCEN

This bit reflects the state of the ring oscillator clock at all times. The 8051 can write this bit to start or stop the ring oscillator. Other hardware events can also start or stop this clock.
= 1 turn on ring oscillator
= 0 turn off ring oscillator
This bit is reset when the 8051 goes into “SLEEP” mode and is set when the 8051 first wakes up from “SLEEP” mode.

KBCLK/ROSC

This bit is used to control the clock source for the 8051.
1 = 8051 clock source is KBCLK
0 = 8051 clock source is ring oscillator.

This bit is reset when the 8051 just wakes up from the “SLEEP” mode

KBDCLK[1:0]

These 2 bits control the 8051 system clock frequencies.

TABLE 82 - KBDCLK CONTROL BIT ENCODING

KBDCLK[1:0] CONTROL BITS KSTP_CLK REGISTER		KBD CLOCK FREQUENCIES
D7	**D6**	**FDC37N972**
0	0	12MHz
0	1	16MHz
1	0	24MHz
1	1	RESERVED

8051 RING OSCILLATOR FAIL-SAFE CONTROLS

A fail-safe control for the 8051 ring oscillator is in the FDC37N972 as protection against unpredicted VCC2 power failures.

The fail-safe ring oscillator sequence occurs as follows:

1. A VCC2 power-fail event is detected when the PWRGD pin changes from “1” to “0” (FIGURE 3 – POWER-FAIL EVENT).

2. The power-fail event sequence starts the 8051 Ring Oscillator. The Ring Oscillator frequency range is the same as the FDC37C95X; i.e., 4MHz to 12MHz.

3. The 8051 system clock is switched to the ring oscillator. NOTE: following a power fail event, VCC2 must be ≥ 3V and the 14.318MHz input clock CLOCKI must remain stable for 10µs min. (FIGURE 4 - VCC2 POWER-UP TIMING).

4. An 8051power-fail interrupt (pfi) is generated to inform the 8051 of the power fail event.

There are four functional power-fail event scenarios. The actions taken for each are described in TABLE 83.

TABLE 83 - POWER-FAIL EVENT ACTIONS

	8051 STATE	ACTIONS			DESCRIPTION
		ASSERT PGI[1]	ASSERT RING OSC.[2]	ASSERT 8051 FLASH ACCESS	
1	SLEEPING ON RING OSC.	✓	-	-	NO FAIL-SAFE ACTIONS TAKEN
2	RUNNING ON RING OSC.	✓	-	-	NO FAIL-SAFE ACTIONS TAKEN; 8051 CAN RESPOND TO PFI IF NEEDED.
3	RUNNING ON PLL	✓	✓	-	INTERNAL PWRGD IS DELAYED UNTIL RING OSC. IS ASSERTED.
4	STOPPED ON PLL	✓	✓	✓	INTERNAL PWRGD IS DELAYED UNTIL RING OSC. IS ASSERTED AND THE 8051 CONTROLS THE FLASH.

NOTE 1: PGI is the Powergood Interrupt bit D0 in the PWRGD_INT register (see Power Fail IRQ on page 184).
NOTE 2: The 8051 is switched to the Ring Oscillator after a delay.

(See PWRGD and VCC1_PWRGD timing is illustrated in FIGURE 3 – POWER-FAIL EVENT through FIGURE 5 - VCC1_PWRGD TIMING)

8051 MEMORY MAP

The FDC37N972 has two modes of ROM support based on the Bondout Option.

Under ALT Bondout, the 8051 can address 2KB of internal ROM, 256B of internal Scratch ROM, and up to 32K of external ROM. When high, the nEA pin is used to enable fetches to the 2K + 256B of internal ROM and when low the nEA pin diables fetches to internal ROM access by routing them to external ROM. The FDC37N972 also contains 256 bytes of internal on-chip RAM.

For ALT Bondout with nEA=1, the internal ROM is addressed from 0-7FF, all ROM access from 800h-7FFFh are invalid address locations. It can support up to 32K bytes of additional external code memory addressed as 8000h to FFFFh by the 8051. This 32K can be mapped to any of the sixteen 32K memory block in the 512K external ROM by the KMEM register.

Under SMSC Bondout, the 8051 can address 256B of internal Scratch ROM and 32K of external ROM. The nEA pin is used to enable access to the 256B of internal Scratch ROM or External program ROM. The FDC37N972 also contains 256 bytes of internal on-chip RAM.

Under SMSC Bondout with nEA=0, all the ROM is addressed as the external ROM. It can support up to 32K bytes of external code memory addressed as 00h to 7FFFh (the addresses from 8000h to FFFFh wrap to the same addresses as 00h to 7FFFh). This 32K can be mapped to any of the sixteen 32K memory blocks in the 512K external ROM by the

KMEM register. At initial power-up (VCC1 POR) the chip will execute from the block selected by the default value of the KMEM register.

The 8051 can access up to 32K bytes of external RAM addressed from 0-7FFFh. Refer to TABLE 86 for a list of the implemented on-chip memory mapped registers. External memory addressed from 8000h-FFFFh will access the 32K bytes of program memory (8000-FFFFh) selected by the KMEM register.

The 256 bytes of RAM from 7E00h-7EFFh as well as the 256 bytes of Scratch RAM from 7D00h-7DFFh are powered by VCC1. These are general purpose Read/Write registers available to the 8051. The Scratch RAM may be converted into scratch ROM by setting the MMC bit.

Memory Map Configuration Control Bit

The Configuration Register 0, an 8051 memory mapped register at address 7FF4h includes a bit called the Memory Map Control bit (MMC). The MMC bit is bit-3 of this register and defaults to zero on VCC1 POR. When MMC=0 the 8051 memory map will contain an additional 256 bytes of external scratch RAM in the address range 7D00h through 7DFFh. When MMC=1 the scratch ram at 7D00h-7DFFh becomes scratch ROM at 00h-0FFh (for an SMSC Bond Out device) or scratch ROM at 800h-8FFh (for an ALT Bond Out device).

The Configuration Register 0 register is described in the 8051 Control Register Section of this specification.

SMSC/ALT Bond Option [nEA=0]

Regardless of the bonding option, if nEA is held low the 8051 memory map for both options is the same as shown in the figure below.

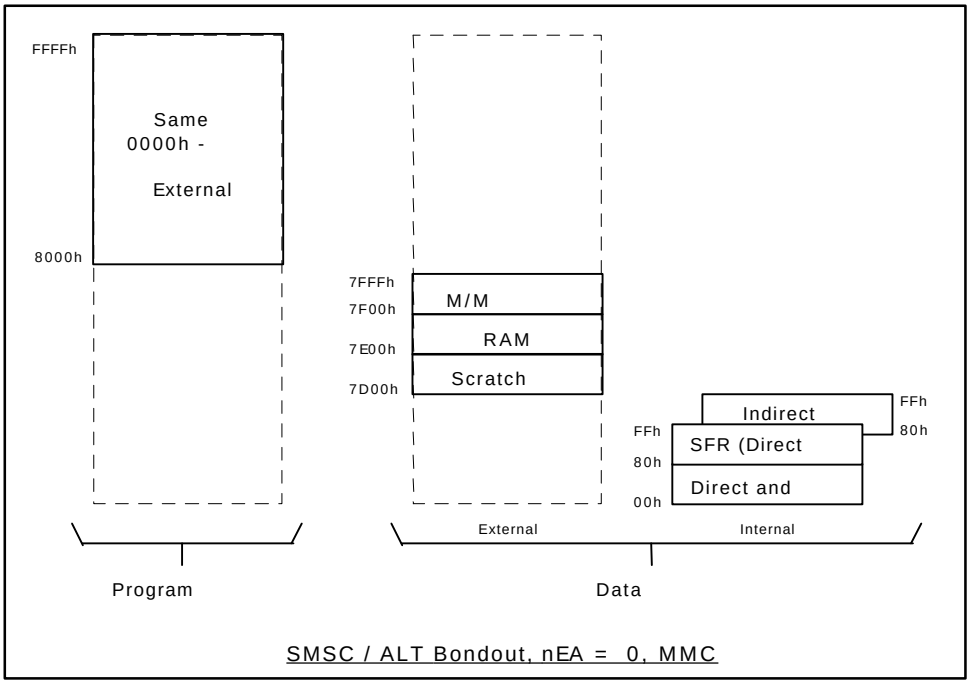


FIGURE 13 - 8051 MEMORY MAP FOR ANY BOND OPTION WITH NEA LOW

Instructions to access memory
MOV : Internal RAM/Registers.
MOVC : Program ROM from 0000h through FFFFh
MOVX : External RAM from 7D00h through 7FFFh -AND-
External ROM from 8000h through FFFFh. (allows flashing of ROM).
SMSC Bond Option [nEA=1]

This section describes the 8051 memory map for an SMSC bonded part where the nEA pin is high. The MMC bit determines the configuration of the 8051's memory map. When nEA=1 an additional 256 of re-writable ROM space can be added to the 8051's internal ROM space to allow patch code upgrades. In order to take advantage of this extra 256 bytes of scratch RAM/ROM certain design considerations must be met as outlined in the following Programmers notes.

MMC bit = 0

When the MMC bit is low (VCC1 POR default) a hard coded long jump LJMP to 8000h is encoded at addresses 00h through 02h and a 256 byte scratch RAM is located at external addresses 7D00-7DFF. The encoding for the hard coded Long Jump is shown in the following table.

HARD CODED LJMP TO 8000H.

8051 Address	Encoding
00h	02h
01h	80h
02h	00h

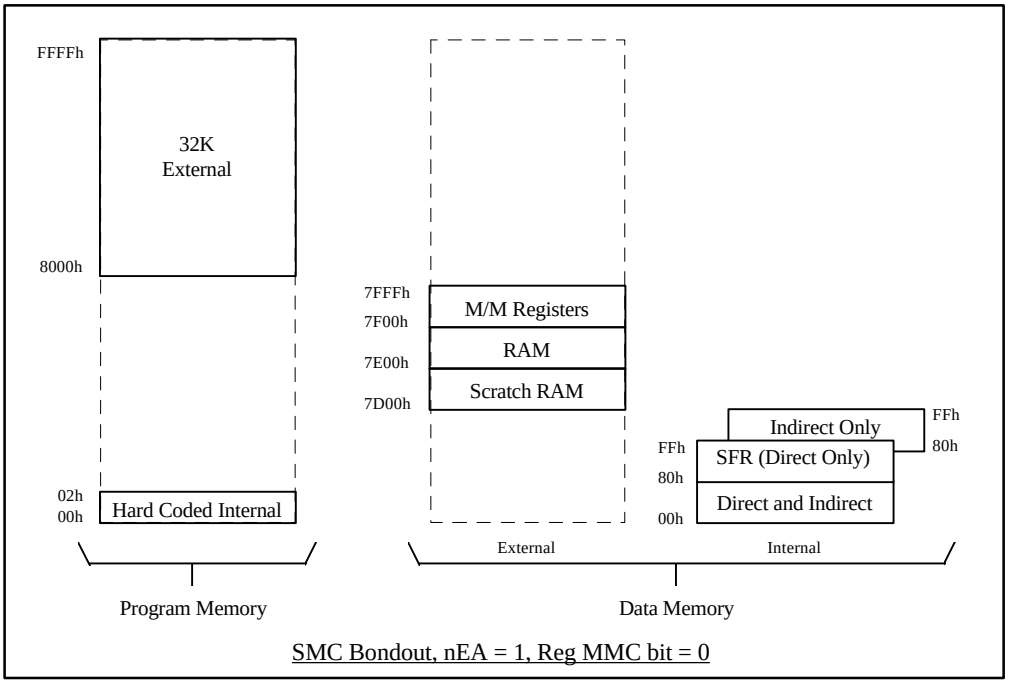


FIGURE 14 - 8051 MEMORY MAP FOR SMC BOND OPTION WITH NEA=1, MMC=0

Instructions to access memory
MOV : Internal RAM/Registers.
MOVC : Program ROM from 8000h through FFFFh
MOVX : External RAM from 7D00h through 7FFFh -AND-
External ROM from 8000h through FFFFh. (allows flashing of ROM).

MMC bit = 1
When the MMC bit is high the scratch RAM at 7D00h-7DFFh is disabled and now becomes the executable internal scratch ROM at address locations 00h-0FFh. The hard coded LJMP to 8000h is overrided by the scratch ROM.

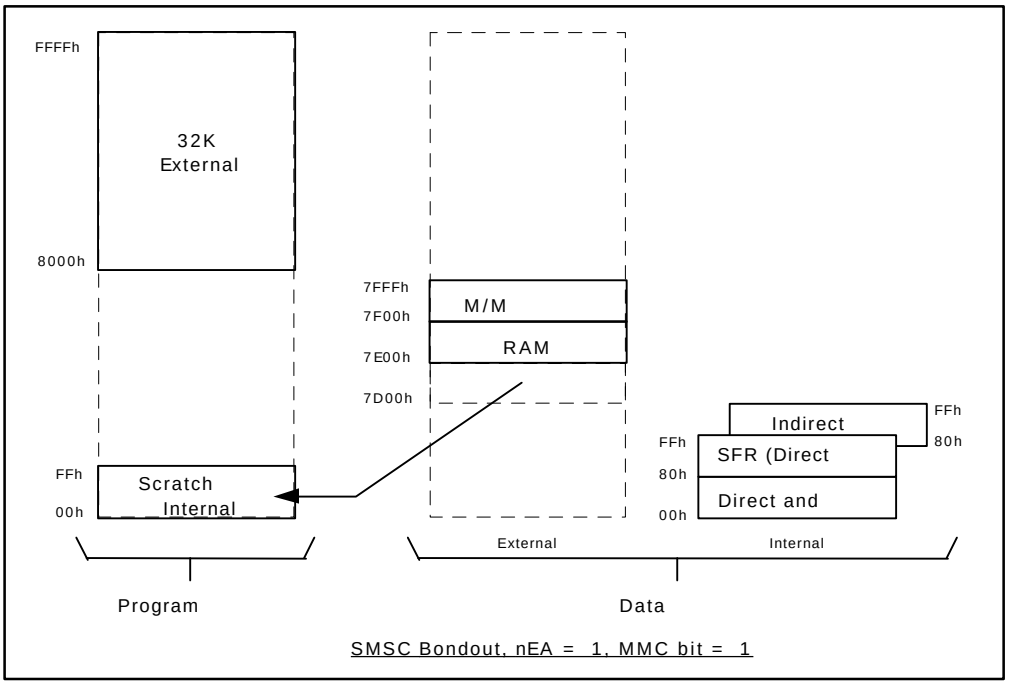


FIGURE 15 - 8051 MEMORY MAP FOR SMC BOND OPTION WITH nEA=1, MMC=1

Instructions to access memory
MOV : Internal RAM/Registers.
MOVC : Program ROM from 8000h through FFFFh called from 00h-0FFh or from 8000h-0FFFFh.
Program ROM from 00h through 0FFh called from 00h-0FFh only.
MOVX : External RAM from 7E00h through 7FFFh -AND-
External ROM from 8000h through FFFFh. (allows flashing of ROM).

ALT Bond Option [nEA=1]
This section describes the 8051 memory map for an ALT bonded part where the nEA pin is high. The MMC bit determines the configuration of the 8051's memory map.

MMC bit = 0
When the MMC bit is low (VCC1 POR default) an additional 256 bytes of Scratch RAM are added to the 8051's memory map at addresses 7D00h though 7DFFh.

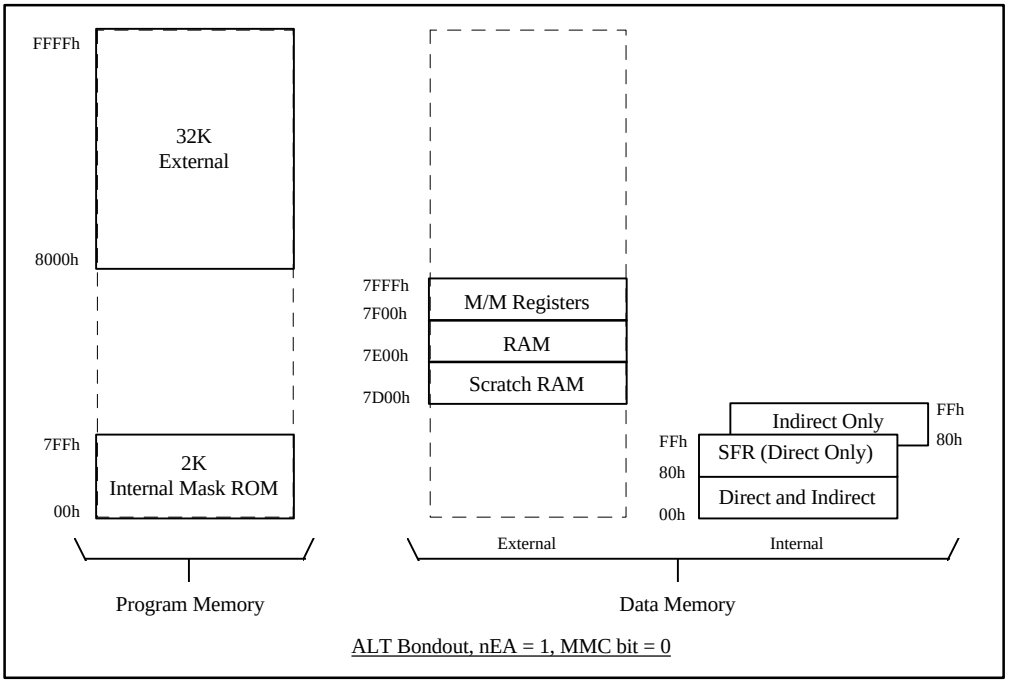


FIGURE 16 - 8051 MEMORY MAP FOR ALT BOND OPTION WITH NEA=1, MMC=0

Instructions to access memory
MOV : Internal RAM/Registers.
MOVC : Program ROM from 8000h through FFFFh called from 00h-7FFh or from 8000h-0FFFFh. Program ROM from 00h through 7FFh called from 00h-7FFh only.
MOVX : External RAM from 7D00h through 7FFFh -AND-
External ROM from 8000h through FFFFh. (allows flashing of ROM).

MMC bit = 1
When the MMC bit is high an additional 256 bytes of executable ROM space between address 800h and 8FFh is added to the 8051's internal ROM space to allow patch code upgrades.

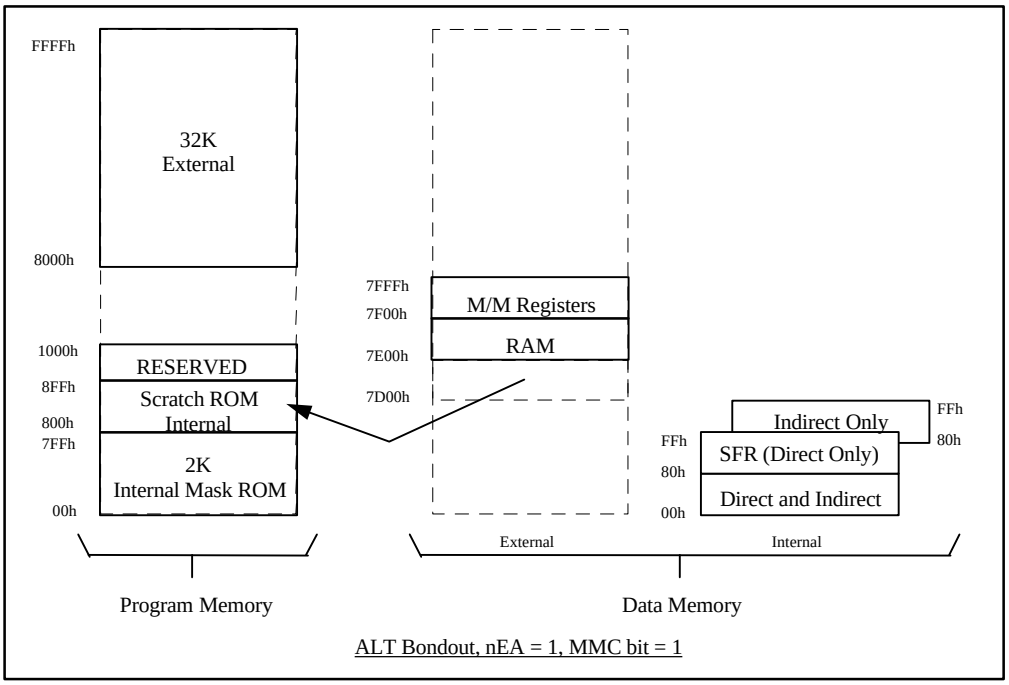


FIGURE 17 - 8051 MEMORY MAP FOR ALT BOND OPTION WITH nEA=1, MMC=1

Instructions to access memory
MOV : Internal RAM/Registers.
MOVC : Program ROM from 8000h through FFFFh called from 00h-8FFh or from 8000h-0FFFFh. Program ROM from 00h through 8FFh called from 00h-8FFh only.
MOVX : External RAM from 7E00h through 7FFFh -AND-
External ROM from 8000h through FFFFh. (allows flashing of ROM).

FLASH ROM INTERFACE

OVERVIEW

The FDC37N972 supports a 512k Byte Flash ROM interface (see HOST BOOT BLOCK SELECT on page 195.) A high-order address bit FA18 is added to the FDC37N972 on GPIO13 (see TABLE 4 for a description of the Alternate Function pins and MULTIFUNCTION PIN on page 271).

A chip enable output nFCS for the Flash ROM interface is '1' when the 8051 is sleeping with control of the Flash or can optionally be configured to follow nFRD (see PROGRAMMABLE FLASH CHIP SELECT on page 196). The external Flash ROM interface timing for the high-performance 8051 core is shown below in FIGURE 18. The preliminary Flash ROM Address read-access times are shown in TABLE 84. (**NOTE: THESE SPECIFICATIONS ARE SUBJECT TO CHANGE**)

TABLE 84 - FLASH ADDRESS ACCESS TIMES

8051 CLOCK (MHz)	FLASH ADDRESS ACCESS TIME (ns)
24	65
16	115
12	165

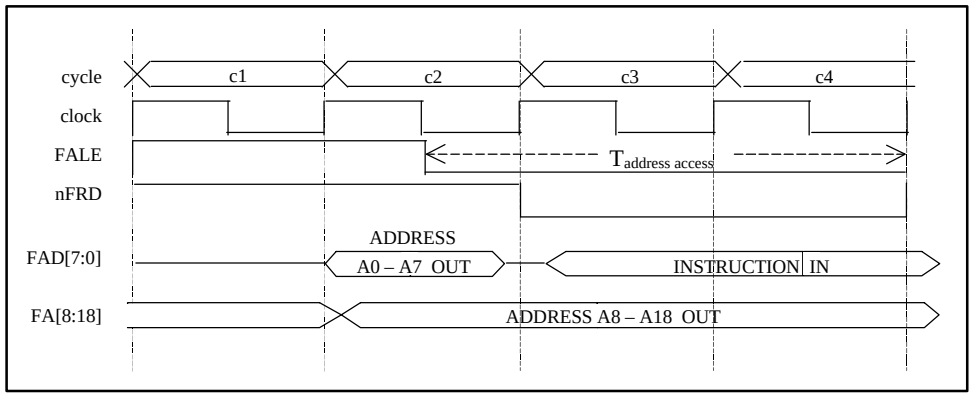


FIGURE 18 - 8051 PROGRAM READ FLASH ROM INTERFACE TIMING

8051 CONTROL REGISTERS

SPECIAL FUNCTION REGISTERS (SFRS)

The high-performance 8051 includes SFRs to support the extended interrupt unit and timer 2 (TABLE 85). The high-performance 8051 does not support the MISZ register.

TABLE 85 - 8051 CONTROL REGISTERS

REGISTER NAME	STARTING ADDRESS	FIX BIT REGISTERS								REGISTER RESET VALUE
		D7	D6	D5	D4	D3	D2	D1	D0	
SP	81H									7H
DPLO	82H									
DPHO	83H									
DPL1(1)	84H									
DPH1(1)	85H									
DPS(1)	86H	0	0	0	0	0	0	0	SEL	
PCON	87H	SMOD0	-	1	1	GF1	GF0	STOP	IDLE	30H
TCON	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	
TMOD	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	
TL0	8AH									
TL1	8BH									
TH0	8CH									
TH1	8DH									
CKCON(1,3)	8EH	-	-	T2M	T1M	T0M	MD2	MD1	MD0	1H
EXIF(1)	91H	IE5	IE4	IE3	IE2	1	0	0	0	8H
MPAGE(1,2)	92H									00H
SCON*	98H	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	
SBUF	99H									
IE	A8H	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	
IP*	B8H	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	
T2CON	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	
RCAP2L	CAH									
RCAP2H	CBH									
TL2	CCH									
TH2	CDH									
PSW	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	
EICON(1)	D8H	SMOD1	1	EPFI	PFI	WDTI	0	0	0	40H
ACC	E0H									

REGISTER NAME	STARTING ADDRESS	FIX BIT REGISTERS								REGISTER RESET VALUE
		D7	D6	D5	D4	D3	D2	D1	D0	
EIE(1)	E8H	1	1	1	EWDI	EX5	EX4	EX3	EX2	E0H
B	F0H									
EIP(1)	F8H	1	1	1	PWDI	PX5	PX4	PX3	PX2	E0H

(1) Not part of standard 8051 architecture. See Appendix B.
(2) The MPAGE special function register provides a means of 16-bit addressing without using the data pointer. During MOVX A, @Ri and MOVX @Ri, A instructions, the 8051 places the contents of the MPAGE register on the upper 8 address bits. The MPAGE register default is '00H'.
(3) The TM2 bit in the CKCON register is available, but not used, when Timer 2 is not implemented (timer =0).

*=Bit-addressable register

MEMORY MAPPED CONTROL REGISTERS (MMCRS)

MMCR SUMMARY

The Memory Mapped Control Registers are on-chip memory-mapped registers that can be accessed by the 8051 but are external to the 8051 core (TABLE 86). The 8051 can access all of the Memory Mapped Control Registers. The 8051 MMCR addresses are described in Column #4 (8051 ADDR) in TABLE 86.

Some MMCRs can also be accessed through the ISA Host interface (ISAxxh), the Mailbox Registers interface (MBXxxh), the Embedded Controller Interface (ECI BASE), and the ACPI PM1 Block Interface (PM1). These addresses are described in Column #2 (SYSTEM ADDRESS) in TABLE 86.

These Memory Mapped Control Registers can be accessed by the following types of 8051 instructions.

```
movx    A,@DPTR
movx    @DPTR,A
mov     MPAGE,#7FH
movx    A,@Rx    (R0 or R1 only)
mov     MPAGE,#7FH
movx    @Rx,A    (R0 or R1 only)
```

TABLE 86 - 8051 ON-CHIP EXTERNAL MEMORY MAPPED REGISTERS

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
Reserved	-	-	F0h	W	VCC1	-			-	7
Host I/F Data Reg [KBD Data/Command Write Reg.]	ISA 60h ISA 64h	W	F1h	R	VCC1	-		Y	205	1,7
Host I/F Data Reg [KBD Data Read Reg.]	ISA 60h	R	F1h	W	VCC1	-		Y	205	7
Host I/F Status Reg [KBD Status Reg.]	ISA 64h	R	F2h	R/W	VCC1	00h		Y	205	2,7
RTC Address 1		R/W	-	-	VCC1	00h			-	13
RTC Data 1		R/W	-	-	VCC1	-			-	13
RTC Address 2		R/W	-	-	VCC1	00h			-	13
RTC Data 2		R/W	-	-	VCC1	-			-	13
HTIMER	-	-	F3h	R/W	VCC1	00h			177	
Config Reg 0	-	-	F4h	R/W	VCC1	00h			163	
RTCCNTRL	-	-	F5h	R/W	VCC1	80h			293	6
RTCADDRL	-	-	F6h	R/W	VCC1	00h			294	
RTCDATAL	-	-	F7h	R/W	VCC1	00			294	
RTCADDRH	-	-	F8h	R/W	VCC1	00h			294	
RTCDATAH	-	-	F9h	R/W	VCC1	00h			294	
Aux Host Data Reg [KBD Data Read Reg.]	ISA 60h	R	FAh	W	VCC1	-		Y	205	3,7
GATEA20	-	-	FBh	R/W	VCC1	01h			210	
FLASH CONFIG.	-	-	FCh	R/W	VCC1	00h	-	-	193	17
PCOBF	-	-	FDh	R/W	VCC1	00h			206	
SETGA20L	-	-	FEh	W	VCC1	-			210	
RSTGA20L	-	-	FFh	W	VCC1	-			210	
Interrupt 0 source register	-	-	00h	R/WC	VCC1	00h			168	
Interrupt 0 mask register	-	-	01h	R/W	VCC1	00h			170	

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
Interrupt 1 source register	-	-	02h	R/WC	VCC1	00h			170	
Interrupt 1 mask register	-	-	03h	R/W	VCC1	00h			171	
Keyboard Scan out	-	-	04h	W	VCC1	20h			215	
Keyboard Scan in	-	-	04h	R	VCC1	-			215	
-	-	-	05h	-	-	-	-	-	-	-
Device Rev register	-	-	06h	R	VCC1	00h			162	
Device ID register (SMSC BONDOUT)	-	-	07h	R	VCC1	0Bh			163	
Device ID register (ALT BONDOUT)	-	-	07h	R	VCC1	0Ah			163	
System-to-8051 Mailbox register 0	MBX 82h	R/W	08h	RC	VCC1	00		Y	248	4
8051-to-system Mailbox register 1	MBX 83h	RC	09h	R/W	VCC1	00		Y	249	5
Mailbox register [2-F]	MBX 84h-91h	R/W	0A-17h	R/W	VCC1	00h		Y	244	
GPIO Direction register A	-	-	18h	R/W	VCC1	00h			262	
GPIO Output register A	-	-	19h	R/W	VCC1	00h			262	
GPIO Input register A	-	-	1Ah	R	VCC1	-			262	
GPIO Direction register B	-	-	1Bh	R/W	VCC1	02h			263	
GPIO Output register B	-	-	1Ch	R/W	VCC1	00h			263	
GPIO Input register B	-	-	1Dh	R	VCC1	-			263	

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
GPIO Direction register C	-	-	1Eh	R/W	VCC1	00h			264	
GPIO Output register C	-	-	1Fh	R/W	VCC1	00h			264	
GPIO Input register C	-	-	20h	R	VCC1	-			264	
LED register	-	-	21h	R/W	VCC1	00h			249	
OUT register D	-	-	22h	R/W	VCC1	00h			265	
OUT register E	-	-	23h	R/W	VCC1	00h			265	
IN register F	-	-	24h	R	VCC1	-			265	
PWM0 register	MBX 92h	R/W	25h	R/W	VCC1	00h		Y	252	
PWM1 register	MBX 93h	R/W	26h	R/W	VCC1	00h		Y	252	
KSTP_CLK	-	-	27h	R/W	VCC1	10h			143	
Fan Control Register	MBX 9D	R/W	28h	R/W	VCC1	30h		Y	253	
KMEM	-	-	29h	R/W	VCC1	00h			188	
WAKEUP Source 1	-	-	2Ah	R/WC	VCC1	00h			172	
WAKEUP Source 2	-	-	2Bh	R/WC	VCC1	00h			173	
WAKEUP mask 1	-	-	2Ch	R/W	VCC1	00h			175	
WAKEUP mask 2	-	-	2Dh	R/W	VCC1	00h			175	
-	-	-	2Eh	-	-	-	-	-	-	-
KSTP_CLK_2	-	-	2Fh	R/W	VCC1	00h	-	-	142	-
Multiplexing 3 register	-	-	30h	R/W	VCC1	00h			272	
ACCESS.BUS Control reg	-	-	31h	W	VCC1	00h			239	
ACCESS.BUS Status reg	-	-	31h	R	VCC1	81h			239	
ACCESS.BUS Own Address reg	-	-	32h	R/W	VCC1	00h			239	
ACCESS.BUS Data reg	-	-	33h	R/W	VCC1	00h			240	
ACCESS.BUS Clock	-	-	34h	R/W	VCC1	00h			240	
-	-	-	35h	-	-	-			-	

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
-	-	-	36h	-	-	-			-	
WDT Control/Status	-	-	37h	R/W	VCC1	00h			184	
WDT Timer	-	-	38h	R/W	VCC1	FFh			184	
-	-	-	39h	-	-	-	-	-	-	-
PP Status Reg		-	3Ah	R/W	VCC2		00h		257	9
PP Control Reg	-	-	3Bh	R/W	VCC2		00h		258	
PP Data Reg	-	-	3Ch	R/W	VCC2		00h		258	
Multiplexing 1 register	-	-	3Dh	R/W	VCC1	00h			266	
Output Enable register			3Eh	R/W	VCC1	see note	see note		164	11
DISABLE register	-	-	3Fh	R/W	VCC1	00h			162	
Multiplexing 2 register	-	-	40h	R/W	VCC1	00h			270	
PS/2 Port1 Control/ PS/2 Chan A Tx/Rx	-	-	41h	R/W	VCC2	-	00h		227	7
PS/2 Port1 Status/ PS/2 Chan A Control	-	-	42h	R R/W	VCC2	-	40h		229	7
PS/2 Port1 Error/ PS/2 Chan A Status	-	-	43h	R	VCC2	-	00h		231	7
PS/2 Port1 Transmit	-	-	44h	W	VCC2	-	00h		232	
PS/2 Port1 Receive/ PS/2 Chan B Tx/Rx	-	-	45h	R R/W	VCC2	-	00h		232	7
PS/2 Chan B Control	-	-	46h	R/W	VCC2	-	40h		220	
PS/2 Chan B Status	-	-	47h	R	VCC2	-	00h		222	
PS/2_ STATUS_2	-	-	48h	R	VCC2	-	00h	-	224	

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
PS/2 Port2 Control/ PS/2 Chan C Tx/Rx	-	-	49h	R/W	VCC2	-	00h		227	7
PS/2 Port2 Status/ PS/2 Chan C Control	-	-	4Ah	R R/W	VCC2	-	40h		229	7
PS/2 Port2 Error/ PS/2 Chan C Status	-	-	4Bh	R	VCC2	-	00h		231	7
PS/2 Port2 Transmit	-	-	4Ch	W	VCC2	-	00h		232	
PS/2 Port2 Receive/ PS/2 Chan D Tx/Rx	-	-	4Dh	R R/W	VCC2	-	00h		232	7
PS/2 Chan D Control	-	-	4Eh	R/W	VCC2	-	40h	-	220	
PS/2 Chan D Status			4Fh	R	VCC2	-	00h		222	
-	-	-	50h-51h	-	-	-	-	-	-	
8051_SIRQ	-	-	52h	R/W	VCC1	00h	-	-	181	
EC_DATA	ECI BASE	R/W	53h	R/W	VCC1	00h		Y	84	12
EC_ COMMAND	ECI BASE+4	W	53h	R/W	VCC1	00h		Y	84	12
EC_STATUS	ECI BASE+4	R	54h	R/W	VCC1	00h		Y	84	12
-	-	-	55h	-	-	-	-	-	-	-
-	-	-	56h	-	-	-	-	-	-	-
Edge Select 4A			57h	R/W	VCC1	00h			178	
Edge Select 4B			58h	R/W	VCC1	00h			178	
Wake up SRC 4			59h	R/WC	VCC1	00h			173	
Wake Up Mask 4			5Ah	R/W	VCC1	00h			176	
-	-	-	5Bh	-	-	-	-	-	-	-

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
Edge Select 5A			5Ch	R/W	VCC1	00h			178	
Edge Select 5B			5Dh	R/W	VCC1	00h			179	
Wake up SRC 5			5Eh	R/WC	VCC1	00h			174	
Wake Up Mask 5			5Fh	R/W	VCC1	00h			176	
-	-	-	60h	-	-	-	-	-	-	-
Edge Select 6A			61h	R/W	VCC1	00h			179	
Edge Select 6B			62h	R/W	VCC1	00h			180	
Wake up SRC 6			63h	R/WC	VCC1	00h			174	
-	-	-	64h-65h	-	-	-			-	
Wake Up Mask 6			66h	R/W	VCC1	00h			177	
ACCESS.BUS 2 Control reg	-	-	67h	W	VCC1	00h			241	
ACCESS.BUS 2 Status reg	-	-	67h	R	VCC1	81h			241	
ACCESS.BUS 2 Own Address reg	-	-	68h	R/W	VCC1	00h			242	
ACCESS.BUS 2 Data reg	-	-	69h	R/W	VCC1	00h			242	
ACCESS.BUS 2 Clock	-	-	6Ah	R/W	VCC1	00h			242	
-	-	-	6Bh – 6Fh	-	-	-	-	-	-	-
Mailbox registers[10-1F]	MBX A0-AF	R/W	70h-7Fh	R/W	VCC1	00		Y	244	
PM1_STS2	PM1+1	R/WC	80h	R/W	VCC1	00		Y	279	
PM1_EN2	PM1+3	R/W	81h	R	VCC1	00		Y	280	
PM1_CNTRL2	PM1+5	R/W	82h	R	VCC1	00		Y	281	
8051_PM_ STS	-	-	83h	R/W	VCC1	00	-	-	282	-
PWRGD_INT	-	-	84h	R/WC	VCC1	00	-	-	180	15

REGISTER NAME	SYSTEM ADDRESS	SYSTEM ADDR. TYPE	8051 ADDR. (7F00+)	8051 TYPE	POWER PLANE	VCC1 POR	VCC2 POR	ZERO WAIT STATE (8)	REF. PAGE#	NOTES
-	-	-	85h-8Dh	-	-	-	-	-	-	-
Test Register	-	-	8Eh-8Fh	-	-	-	-	-	-	-
-	-	-	90h-EFh	-	-	-	-	-	-	-
256 bytes of RAM	-	-	7E00-7EFFh	R/W	VCC1				146	

Notes:
1. Although the Input and Output Data registers are physically separate, they share address 7FF1.
2. The 8051 CPU cannot write to some bits of the Status register.
3. Writing to the Auxiliary Output Data Register, loads the Output data register and can set the AUXOBF1 output if enabled. This does not set the PCOBF output.
4. Interrupt is cleared when read by the 8051.
5. Interrupt is cleared when read by the host.
6. See RTC control Register Definition.
7. These addresses are shared between the PS/2 Devil Logic and the SMSC PS/2 Hardware Channels A – D (see PS/2 DEVICE INTERFACE section on page 221).
8. When accessed for a read or write by the System the registers marked with a “Y” will drive the Zero wait state pin active.
9. Bit 0 is the only writable or resetable bit in this register.
10. When IRESET_OUT is cleared (written from “1” to”0”) 8051STP_CLK bit D0 as well as HMEM bits D1 and D0 are all set to “1”.
11. VCC1 POR = 00000X10b, VCC2 POR = 00000X1Xb where X is not affected by VCC2 POR, but is left at the current value.
12. These registers have the same structure as the keyboard interface registers.
13. The ISA RTC registers are relocatoable and accessed by the 8051 through MMCRs 0x7FF5 – 0x7FF9.
14. See Section General Purpose I/O (GPIO) on page 265.
15. See **Power Fail IRQ** on page 184.
16. See FLASH CONFIGURATION REGISTER on page 197.
17. SMSC PS/2 Status_2 REGISTERS section on page 229.

8051 CONFIGURATION/CONTROL MEMORY MAPPED REGISTERS

DISABLE REGISTER

TABLE 87 - DISABLE REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F3F	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	Parallel Port 1 = Enable 0 = Disable	Serial Port 1 = Enable 0 = Disable	IR Port 1 = Enable 0 = Disable	Floppy Port 1 = Enable 0 = Disable	UD[1]	SYSTEM FLASH Interface 1=Enable 0= DISABLE	Re-ser-ved	FORCE WRTPRT[2]

NOTE[1] The UD bits are User-Defined. UD bits are maintained by 8051 software, only.
NOTE[2] See Section FDC FORCE WRITE PROTECTION page 84 for a description of the FORCE WRTPRT Bit function.

DEVICE REV REGISTER

By reading this register, 8051 firmware can confirm the device revision that it is running on.

TABLE 88 - DEVICE REV REGISTER

Host	N/A
8051	0x7F06 (R)
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R	R	R	R	R	R	R	R	R
Bit Description	Current Revision							1

This register is hardwired.

DEVICE ID REGISTER

By reading this register, 8051 firmware can determine which device it is running on.

TABLE 89 - DEVICE ID REGISTER

Host	N/A
8051	0x7F07 (R)
Power	VCC1
Default	0x0A

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R	R	R	R	R	R	R	R	R
Bit description	0	0	0	0	0	1	1	1

CONFIGURATION REGISTER

TABLE 90 - CONFIGURATION REGISTER 0

Host	N/A
8051	0x7FF4
Power	VCC1
Default	0x00

D7	D6	D5	D4	D3	D2	D1	D0
AUXH	0	OBFEN	PS2_SEL	MMC	PCOBFEN	SAEN	SLEEPFLAG

AUXH

Aux in Hardware; When high, AUXOBF of the status register is set in hardware by a write to 7FFAh. When low, AUXOBF of the status register is a user defined bit (UD) and R/W.

OBFEN

When set PCOBF is gated onto KIRQ and AUXOBF1 is gated onto MIRQ. When low, KIRQ and MIRQ are driven low. Software should not change this bit when OBF of the status register is equal to 1.

MMC

Memory Map Control Bit : When MMC=0, a 256 Byte Scratch RAM area at 7D00h is available to the 8051. When MMC=1 the Scratch RAM at 7D00h-7DFFh becomes scratch ROM at 00h--FFh.

PCOBFEN

When high, PCOBF reflects whatever value was written to the PCOBF firmware latch assigned to 7FFDH. When low, PCOBF reflects the status of writes to 7FF1H (the output data register).

PS2_SEL

If PS2_SEL=0 (default) then the PS2 Device Interface Logic (DEVIL) is enabled and if PS2_SEL=1 then the SMSC PS2 Interface (SPS2) is enabled. The following table illustrates this:

PS2_SEL	Internal active PS/2 Logic Block
0	PS2 Device Interface Logic (DEVIL)
1	SMSC PS2 Interface Logic (SPS2)

SAEN

Software-assist enable. When set to "1" SAEN allows control of the GATEA20 signal via firmware. If SAEN is reset to '0', GATEA20 corresponds to either the last host-initiated control of GATEA20 or the firmware write to 7FFEh or 7FFFh.

SLEEPFLAG

If SLEEPFLAG="0" when PCON bit-0 is set, the 8051 enters "IDLE" mode, whereas if SLEEPFLAG="1" when PCON bit 0 is set the 8051enters "SLEEP" mode. This bit is cleared by the occurrence of any wake-up events and on VCC1 POR.

OUTPUT ENABLE REGISTER

Table 91 - Output Enable Register

Host	N/A
8051	0x7F3E
Power	VCC1
Default	**00000X10b** on VCC1 POR **00000X1Xb** on VCC2 POR

Output Enable Register VCC1 POR = 0x00000X10, VCC2 POR = 00000X1***X***b where ***X*** means the bit holds its setting preceding VCC2 POR.

	D7-D4	**D3**	**D2**	**D1**	**D0**
8051 AR	R/W	R/W	R	R/W	R/W
	Reserved 0	iRESET_ OVRD	Power_Good	iRESET_OUT	32kHz Output

AR= Access Rights

iRESET_OUT

When POWERGOOD=1, iRESET_OUT is controlled by the 8051.

When POWERGOOD=0, iRESET_OUT is forced high (within 100nsec) and latched. The nRESET_OUT pin is not driven until VCC2 is applied. iRESET_OUT cannot be cleared by the 8051 until POWERGOOD=1.

POWER_GOOD

The Power_Good bit D2 reflects the state of the FDC37N972 VCC2 Power Good pin PWRGD. The Power_Good bit is read-only.

iRESET_OVRD

iRESET Override - when cleared the iRESET_OUT bit functions as described above. When set, iRESET_OUT is given direct control over the internal reset and nRESET_OUT pins without requiring the STOP_CLK counter or affecting the 8051STP_CLK bit or the HMEM register. In the override mode, setting iRESET_OUT drives nRESET_OUT low and clearing iRESET_OUT drives nRESET_OUT high.

The RESET_OUT Override function allows the 8051 to take the rest of the FDC37N972 chip (SIO) out of reset without giving up control (i.e., without stopping its clock and giving the flash interface to the Host).

On the current FDC37N972, nRESET_OUT is driven high by this sequence of events.

Sets STP_CNT to a non-zero value
Clears iRESET_OUT bit, causing
8051STP_CLK bit 0 to get set
HMEM[7:0] to get set to 0x07
and STOP Counter to start decrementing

When STP_CNT reaches 0 the nRESET_OUT pin deasserts (goes high) at which point the 8051's clock stops and the Host owns the Flash Interface.

The above sequence provides a means for the 8051 to directly control the state of the Super I/O block's internal reset. The FDC37N972 provides a means for the 8051 to drive low or toggle the chip's internal reset without stopping the 8051 clock or giving the Flash interface to the host.

32kHz OUTPUT

The 32kHz Output bit D0 controls the FDC37N972 32kHz Output Clock pin 32kHz_OUT. When 32kHz Output is '0', the 32kHz Output Clock is disabled and the 32kHz_OUT pin is driven low. When 32kHz Output is '1', the 32kHz Output Clock is enabled. The 32kHz Output bit is R/W and disabled by default following VCC1 POR.

8051 INTERRUPTS

8051 INTERRUPT ARCHITECHTURE FEATURES

The eleven 8051 core interrupts are shown described in TABLE 92 - 8051 INTERRUPTS. The 8051 has the following run time sources: int0, int1, int2, int3 and int4.

The Interrupt sources of Int5_n create 8051 Wakeup Events which are used to monitor and altar the power management state. There are three type of source triggers for wakeup event: Nonprogrammable (fixed edge), Selectable Edge (SE), Either Edge (EE).

The 8051 core has three interrupt priority levels: PFI, high and low. The PFI interrupt, if enabled, has priority over all other interrupts.

8051 INTERNAL PARALLEL INTERRUPTS

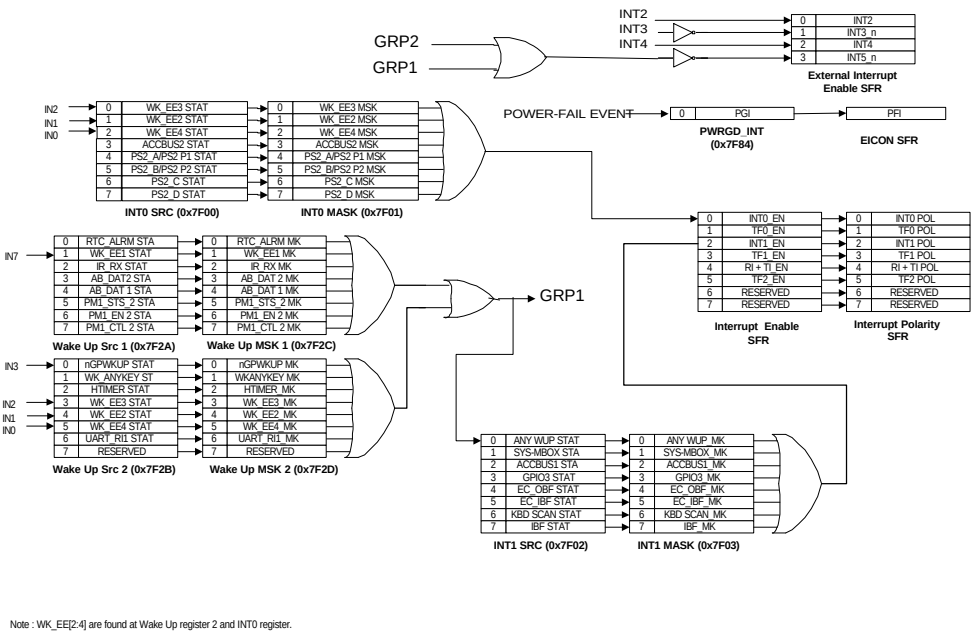


FIGURE 19 - 8051 INTERRUPTS

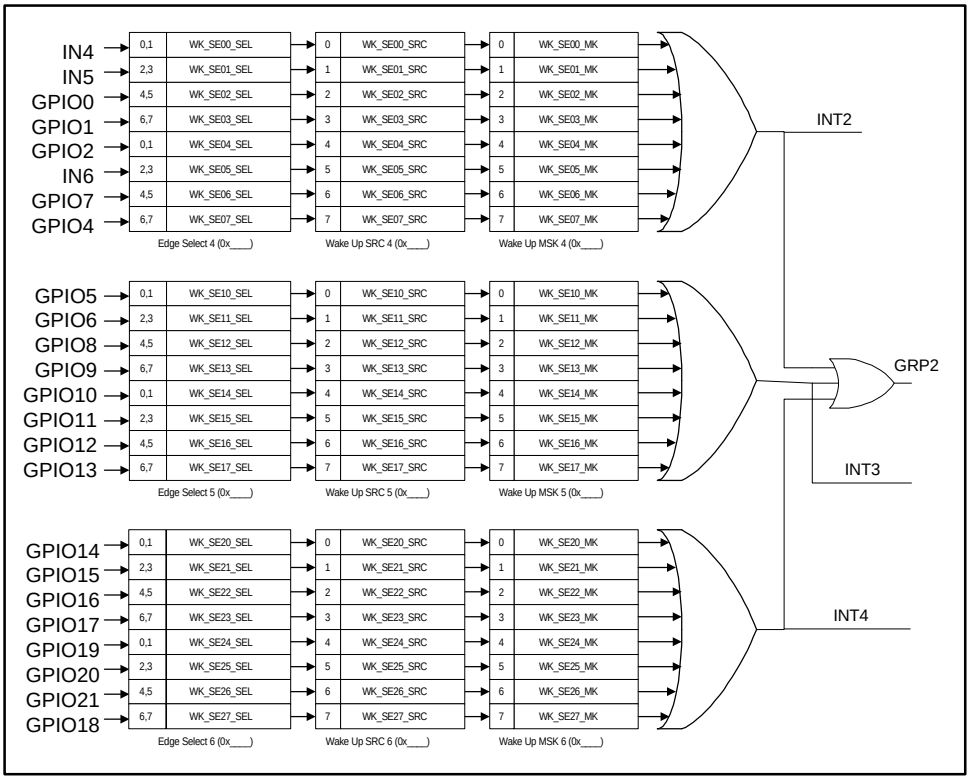


FIGURE 20 - EXTENDED INTERRUPTS & WAKE EVENTS

NOTE: Wake events apply per pin and are available to all functions of that pin. For example, if the IRRX function is selected as an alternate function of the GPIO8 pin (MISC7 = 1), the WK_SE12 event can be used for IR wake-up. See Section 8051 System Power MANAGEMENT on page 198.

TABLE 92 - 8051 INTERRUPTS

INTER-RUPT	DESCRIPTION	NATURAL PRIORITY	INTERRUPT VECTOR	FLAG	ENABLE	PRIORITY CONTROL
pfi	Power Fail Interrupt	0	0x33	EICON.4	EICON.5	n/a
int0_n	External Interrupt 0	1	0x03	TCON.1	IE.0	IP.0
TF0	Timer 0 Interrupt	2	0x0B	TCON.5	IE.1	IP.1
int1_n	External Interrupt 1	3	0x13	TCON.3	IE.2	IP.2
TF1	Timer 1 Interrupt	4	0x1B	TCON.7	IE.3	IP.3
TI_0 or RI_0	Serial Port 0 Transmit or Receive	5	0x23	SCON0.0 (RI_0), SCON0.1 (RI_0)	IE.4	IP.4
TF2 or EXF2	Timer 2 Interrupt	6	0x2B	T2CON.7 (TF2), T2CON.6 (EXF2)	IE.5	IP.5
	RESERVED	7	0x3B	RESERVED	IE.6	IP.6
int2	External Interrupt 2	8	0x43	EXIF.4	EIE.0	EIP.0
int3_n (1)	External Interrupt 3	9	0x4B	EXIF.5	EIE.1	EIP.1
int4	External Interrupt 4	10	0x53	EXIF.6	EIE.2	EIP.2
int5_n	External Interrupt 5	11	0x5B	EXIF.7	EIE.3	EIP.3
	RESERVED	12	0x63	EICON.3	EIE.4	EIP.4

NOTE: The int5_n interrupt is used to restart the 8051 from sleep mode. This interrupt includes the interrupt WAKE UP sources from GRP1 and GRP2 on **FIGURE 19** and **FIGURE 20**.

8051 INT0 SOURCE REGISTER

The eight interrupts in the INT0 Source register (TABLE 93) are logically 'OR'ed to drive the 8051 external interrupt 0 input, int0_n (FIGURE 19). When any bit in the INT0 Source register is '1', an interrupt has occurred and, assuming the interrupt is enabled, the 8051 int0_n input is asserted.

The bits in the INT0 Source register are cleared by a writing a "1" to the bit.

TABLE 93 - 8051 INT0 SOURCE REGISTER

HOST ADDRESS	n/a
8051 ADDRESS	0x7F00
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT NAME	PS2_D	PS2_C	PS2_B/ PS2 P2	PS2_A/ PS2 P1	ACCESS BUS 2	WK_EE4	WK_EE2	WK_EE3

SMSC PS/2 C & D Interrupts – D[7:6]

INT0 Source register bit D7 is the SMSC PS/2 Channel D interrupt; INT0 Source register bit D6 is the SMSC PS/2 Channel C interrupt. These interrupts are active when the PS2_SEL Control bit D4 in Configuration Register 0 (0x7FF4) is '1.'

When the SMSC PS/2 channels are active the PS2_D interrupt is associated with the PS2CLK and PS2DAT alternate functions of the GPIO20 and GPIO21 pins; PS2_C is associated with the IMCLK and IMDATA pins.

Dual-Mode SMSC/DEVIL Interrupts – D[5:4]

INT0 Source register bits D5 and D4 are multiplexed between the SMSC PS/2 Channels A and B and the Devil Logic Ports P1 and P2.

When the PS2_SEL Control bit D4 in Configuration Register 0 (0x7FF4) is '1,' the SMSC PS/2 Interrupt Channels A and B are selected; when PS2_SEL = '0,' the Devil Logic Ports P1 and P2 are selected.

When the SMSC PS/2 channels are active the PS2_B interrupt is associated with the KCLK and KDAT pins; PS2_A is associated with the EMCLK and EMDATA pins.

Access Bus 2 Interrupt – D3

"1" Indicates an ACCESS.bus 2 interrupt is active.

WK_EE[4:2]

ACCESS Bus 2 wake events can be generated. AB_DAT ACCESS BUS 2 bit in Wake Sources (Register 1.)
8051 INT0 Mask Register

The eight interrupts in the INT0 Source register (TABLE 93) are enabled by bits of the same name in the INT0 Mask register (TABLE 94).

When any bit in the INT0 Mask register is '0', the interrupt is enabled. When any bit in the INT0 Mask register is '1, the interrupt is masked. When masked interrupts are asserted, the interrupt will be visible in the interrupt source register but will not assert an interrupt to the 8051.

The bits in the INT0 Mask register are read/write. The INT0 interrupts are enabled by default.

8051 INT0 MASK REGISTER

TABLE 94 - 8051 INT0 MASK REGISTER

HOST ADDRESS	n/a
8051 ADDRESS	0x7F01
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	PS2_D	PS2_C	PS2_B/ PS2 P2	PS2_A/ PS2 P1	ACCESS BUS 2	WK_EE4	WK_EE2	WK_EE3

8051 INT1 Source Register

The eight interrupts in the INT1 Source register (TABLE 95) are logically 'OR'ed to drive the 8051 external interrupt 1 input, int1_n (FIGURE 19).

When any bit in the INT1 Source register is '1', an interrupt has occurred and, assuming the interrupt is enabled, the 8051 int1_n input is asserted.

Bits D0 and D2 – D6 in the INT1 Source register are cleared by a writing a "1" to the bit.

TABLE 95 - 8051 INT1 SOURCE REGISTER

HOST ADDRESS	N/a
8051 ADDRESS	0x7F02
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R**	**R/WC**
BIT NAME	IBF[1]	KBD SCAN	EC_IBF[2]	EC_OBF[3]	GPIO3	ACCESS BUS 1	SYS-MBOX[4]	ANY WUP

ACCESS BUS 1 [D2]
When ACCESS BUS 1 bit is equal to 1 an Access Bus IRQ is active.

IBF [D7]
IBF interrupt bit D7 is set when the host writes to the KBD Data/Command Write register and is cleared when the 8051 reads from that register.

EC_IBF [D5]
EC_IBF interrupt bit D5 is set when the host writes to the EC Command or Data port (see IBF Bit – D1 on page 88).

EC_OBF [D4]
EC_OBF interrupt bit D4 is asserted when the OBF bit in the EC Status register has been cleared (see OBF Bit – *D0* on page 88).

SYS-MBOX [D1]
SYS-MBOX interrupt bit D1 is set when the host writes to mailbox register 0. The bit is cleared when mailbox register 0 is read (see The SYSTEM/8051 Interface Registers on page 252).
8051 INT1 Mask Register

The eight interrupts in the INT1 Source register (TABLE 95) are enabled by bits of the same name in the INT1 Mask register (TABLE 96).

When any bit in the INT1 Mask register is '0', the interrupt is enabled. When any bit in the INT1 Mask register is '1', the interrupt is masked. When masked interrupts are asserted, the interrupt will be visible in the interrupt source register but will not assert an interrupt to the 8051.

The bits in the INT1 Mask register are read/write. The INT1 interrupts are enabled by default.

8051 INT1 MASK REGISTER

TABLE 96 - 8051 INT1 MASK REGISTER

HOST ADDRESS	n/a
8051 ADDRESS	0x7F03
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	IBF	KBD SCAN	EC_IBF	EC_OBF	GPIO3	ACCESS BUS 1	SYS-MBOX	ANY WUP

8051 WAKEUP SOURCE REGISTERS

TABLE 97 - WAKEUP SOURCE REGISTER 1

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2A
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**
BIT NAME AND DESCRIP-TION	1= PM1 CTL 2	1= PM1 EN 2	1= PM1 STS 2	1 = AB_DAT ACCESS. BUS interrupt asserted	1 = AB_DAT ACCESS. BUS 2 interrupt asserted	1 = IRRX (Note 3)	1 = WK_ EE1 changed (Note 1)	1 = RTC_ ALRM asserted (Note 2)

Res = Reserved. Read returns 0, writes are ignored.
Note 1: Input is going from low to high or from high to low (read the GPIO register to find out the value of pin)

AB_DAT1 and AB_DAT2 -- When ACCESS.BUS=1, a start condition or other event was detected on the ACCESS.BUS bus. When ACCESS.BUS 2=1, a start condition or other event was detected on the ACCESS.BUS 2 bus

PM1_STS2, PM1 EN2, PM1CTL2 interrupts: These are set when the corresponding PM1 register has been written by the host.
Note 2: The RTC_ALRM Wake-up is an internally generated Low-to-High edge, produced when the RTC time updates to match the Time Of Day (TOD) alarm setting. This edge will set bit D0 of Wake-up Source 1 Register. Bit D0 will remain set and will only be reset on a read of Wake-up Source 1 Register. If the Wake-up source register is read before the clock has updated (i.e., RTC still equals the TOD alarm) bit D0 is reset and stays reset until the next occurrence of a RTC_ALRM Wake-up event.
Note 3: Wake event is asserted when only when both V_{CC2} is active and IRRX input changes from high to low.
Note 4: The interrupt source bits in this register are cleared by a writing a “1” to the bit.

TABLE 98 - WAKEUP SOURCE REGISTER 2

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2B
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**
BIT NAME AND DES-CRIPTION	RES	1 = UART_RI1 asserted	1= WK_EE4	1 = WK_EE2 transition (both edges)	1 = WK_EE3 transition (both edges)	1 = HTIMER timeouts	1 = WK_ANYKEY is asserted	1= nGPWKUP is asserted

HTIMER Interrupt When HTIMER=1, the hibernation timer counted down to zero.
Note 1: Anykey Wake-up (WK_ANYKE– -- When unmasked, the WK_ANYKEY will wake the 8051 from the “SLEEP” state when any of the Keyboard Scan In (KSI) pins goes low. The Boolean equation below defines the WK_ANYKEY function.
WK_ANYKEY = !(KSI0 & KSI1 & KSI2 & KSI3 & KSI4 & KSI5 & KSI6 & KSI7)

NOTE: The interrupt source bits in this register are cleared by a writing a “1” to the bit.

TABLE 99 - WAKEUP SOURCE REGISTER 4

HOST ADDRESS	N/A
8051 ADDRESS	0x7F59
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**
BIT NAME AND DES-CRIPTION	1 = WK_SE07 asserted	1 = WK_SE06 asserted	1 = WK_SE05 asserted	1 = WK_SE04 asserted	1 = WK_SE03 asserted	1 = WK_SE02 asserted	1 = WK_SE01 asserted	1 = WK_SE00 asserted

Note : The bits in this register are cleared on a WRITE OF “1” TO THE CORRESPONDING BIT.

TABLE 100 - WAKEUP SOURCE REGISTER 5

Host address	N/A
8051 ADDRESS	0x7F5E
POWER	VCC1
DEFAULT	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**
BIT NAME AND DESCRIPTION	1 = WK_SE17 asserted	1 = WK_SE16 asserted	1 = WK_SE15 asserted	1 = WK_SE14 asserted	1 = WK_SE13 asserted	1 = WK_SE12 asserted	1 = WK_SE11 asserted	1 = WK_SE10 asserted

Note : the bits in this register are cleared on a WRITE OF “1” TO THE CORRESPONDING BIT.

TABLE 101 - WAKEUP SOURCE REGISTER 6

Host address	N/A
8051 ADDRESS	0x7F63
POWER	VCC1
DEFAULT	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**	**R/WC**
BIT NAME AND DESCRIPTION	1 = WK_SE27 asserted	1 = WK_SE26 asserted	1 = WK_SE25 asserted	1 = WK_SE24 asserted	1 = WK_SE23 asserted	1 = WK_SE22 asserted	1 = WK_SE21 asserted	1 = WK_SE20 asserted

Note : The bits in this register are cleared on a WRITE OF “1” TO THE CORRESPONDING BIT.

TABLE 102 - WAKEUP MASK REGISTER 1

HOST ADDRESS	N/A
8051 ADDRESS	0x7F2C
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME AND DESCRIPTION	1 = Mask PM1 CTL2	1 = Mask PM1 EN2	1 = mask PM1 STS2	1 = mask AB_DATA ACCESS BUS 1	1 = mask AB_DATA ACCESS. BUS 2	1 = MASK IRRX	1=Mask WK_EE1	1 = Mask RTC_ ALARM

TABLE 103 - WAKEUP MASK REGISTER 2

Host address	N/A
8051 ADDRESS	0x7F2D
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME AND DESCRIPTION	RESERVED	1=mask UART_RI1	1=Mask WK_EE4	1 = Mask WK_EE2	1 = Mask WK_EE3	1 = Mask HTIMER	1 = Mask WK_ANYKEY	1= mask nGPWKUP

TABLE 104 - WAKEUP MASK REGISTER 4

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5A
POWER	VCC1
DEFAULT	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME AND DESCRIPTION	1 = mask WK_ SE07	1 = mask WK_ SE06	1 = mask WK_ SE05	1 = mask WK_ SE04	1 = mask WK_ SE03	1 = mask WK_ SE02	1 = mask WK_ SE01	1 = mask WK_ SE00

TABLE 105 - WAKEUP MASK REGISTER 5

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5F
POWER	VCC1
DEFAULT	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
HOST TYPE	-	-	-	-	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME AND DESCRIPTION	1 = mask WK_S E17	1 = mask WK_ SE16	1 = mask WK_ SE15	1 = mask WK_ SE14	1 = mask WK_ SE13	1 = mask WK_ SE12	1 = mask WK_ SE11	1 = mask WK_ SE10

TABLE 106 - WAKEUP MASK REGISTER 6

HOST ADDRESS	N/A
8051 ADDRESS	0x7F66
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE					-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME AND DESCRIPTION	1 = mask WK_ SE27	1 = mask WK_ SE26	1 = mask WK_ SE25	1 = mask WK_ SE24	1 = mask WK_ SE23	1 = mask WK_ SE22	1 = mask WK_S E21	1 = mask WK_SE 20

8051 HIBERNATION TIMER REGISTER

TABLE 107 - HTIMER REGISTER

Host	N/A
8051	0x7FF3
Power	VCC1
Default	0x00

Hibernation Timer - This 8 bit binary count-down timer can be programmed for from 30 seconds to 128 minutes in 30 second increments. When it expires (reaches “0”), it stops (remains at “0”) and causes a hardware event that will wake up the 8051. This timer is clocked by the 32 KHz clock and is powered by VCC1. Writing a non-zero value to this register starts the counter from that value.

8051 EDGE SELECT REGISTERS

Selectable Edge interrupts

Selectable interrupts SE00-SE07 are on External INT2.
Selectable interrupts SE10-SE17 are on External INT3.
Selectable interrupts SE20-SE27 are on External INT4.

TABLE 108 - EDGE SELECT 4A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F57
POWER	VCC1
DEFAULT	0x00

	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	
BIT NAME AND DESCRIPTION	SE03 Select	SE02 Select	SE01 Select	SE00 Select

TABLE 109 - EDGE SELECTION

Edge Selection Table	D7:6 D5:4 D3:2 D1:0
EDGE High to low	00
Edge Low to High	01
Either Edge	10
Reserved	11

TABLE 110 - EDGE SELECT 4B

HOST ADDRESS	N/A
8051ADDRESS	0x7F58
POWER	VCC1
DEFAULT	0x00

	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	
BIT NAME AND DESCRIPTION	SE07 Select	SE06 Select	SE05 Select	SE04 Select

Refer to **TABLE 109 - EDGE SELECTION** for the edge selection table

TABLE 111 - EDGE SELECT 5A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5C
POWER	VCC1
DEFAULT	0x00

	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	
BIT NAME AND DESCRIPTION	SE13 Select	SE12 Select	SE11 Select	SE10 Select

Refer to **TABLE 109** for the edge selection table.

TABLE 112 - EDGE SELECT 5B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F5D
POWER	VCC1
DEFAULT	0x00

	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	
BIT NAME AND DESCRIPTION	SE17 Select	SE16 Select	SE15 Select	SE14 Select

Refer to **TABLE 109** for the edge selection table.

TABLE 113 - EDGE SELECT 6A

HOST ADDRESS	N/A
8051 ADDRESS	0x7F61
POWER	VCC1
DEFAULT	0x00

	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	
BIT NAME AND DESCRIPTION	SE23 Select	SE22 Select	SE21 Select	SE20 Select

Refer to **TABLE 109** for the edge selection table.

TABLE 114 - EDGE SELECT 6B

HOST ADDRESS	N/A
8051 ADDRESS	0x7F62
POWER	VCC1
DEFAULT	0x00

	D7:6	D5:4	D3:2	D1:0
HOST TYPE	-	-	-	-
8051 R/W	**R/W**	**R/W**	**R/W**	
BIT NAME AND DESCRIPTION	SE27 Select	SE26 Select	SE25 Select	SE24 Select

Refer to **TABLE 109** for the edge selection table.

POWER FAIL IRQ

The PWRGD_INT register (TABLE 115) contains the Power Good Interrupt (PGI) bit, D0. When PGI = '1', the (VCC2) PWRGD input has been deasserted; otherwise, PGI = '0'. **NOTE:** PGI is not asserted when PWRGD is asserted.

The PGI bit is the source for the high-performance 8051 Power Fail Interrupt (pfi) input (FIGURE 19). The VCC2 power fail detect function is implemented as described in 8051 RING OSCILLATOR FAIL-SAFE CONTROLS on page 147.

The PGI bit is readable and is cleared by writing a '1' to D0 in the PWRGD_INT register.

TABLE 115 - POWER GOOD INTERRUPT REGISTER (PWRGD_INT)

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F84	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R/WC**
BIT NAME	RESERVED							PGI

8051 External Serial IRQ Generation

The 8051 can assert an interrupt on the serial IRQ stream to support software-generated SCI, SMI, or PME events (FIGURE 21).

FIGURE 21
NOTE: The 8051 External Serial IRQ is generated and cleared by software.

The 8051 External Serial IRQ interface is controlled by the 8051_SIRQ register (TABLE 116).

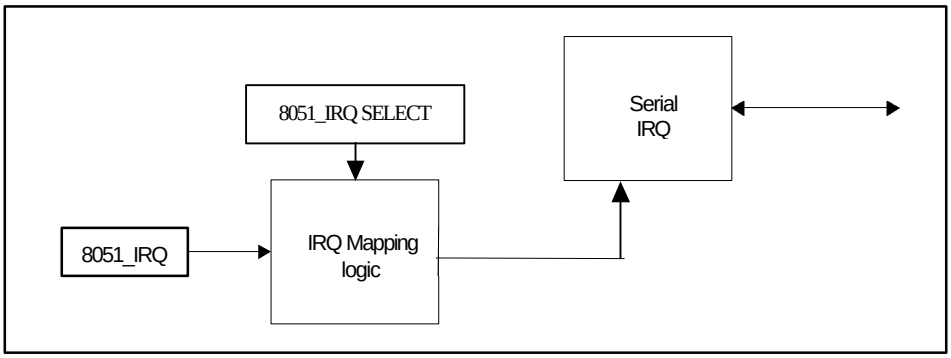


FIGURE 21 - 8051 EXTERNAL SERIAL IRQ BLOCK DIAGRAM

TABLE 116 - 8051_SIRQ REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F52	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R	R
BIT NAME	8051_IRQ SELECT				8051_IRQ ENABLE	8051_IRQ	RESERVED	

8051_IRQ SELECT

Four bits that selects which IRQ is utilized when an interrupt occurs. See **TABLE 117 - 8051 IRQ MAPPING CONTROL BITS**

8051_IRQ ENABLE

This bit must be set to one in order for an interrupt to occur.

8051 IRQ
This bit must set to one in order for the 8051 to assert the mapped interrupt request corresponding to the 8051_IRQ SELECT bits. The defualt state for a disabled IRQ is asserted.

TABLE 117 - 8051 IRQ MAPPING CONTROL BITS

8051_IRQ ENABLE	8051_IRQ SELECT	DESCRIPTION
0	XXXX	DISABLED
1	0000	NO INTERRUPT
1	0001	MAP TO IRQ1
1	0010	MAP TO IRQ2
1	0011	MAP TO IRQ3
1	0100	MAP TO IRQ4
1	0101	MAP TO IRQ5
1	0110	MAP TO IRQ6
1	0111	MAP TO IRQ7
1	1000	MAP TO IRQ8
1	1001	MAP TO IRQ9
1	1010	MAP TO IRQ10
1	1011	MAP TO IRQ11
1	1100	MAP TO IRQ12
1	1101	MAP TO IRQ13
1	1110	MAP TO IRQ14
1	1111	MAP TO IRQ15

WATCH DOG TIMER

WDT OPERATION

When enabled, the Watch Dog Timer (WDT) circuit will generate a system reset if the user program fails to reload the watchdog timer (WDT) within a specified length of time known as the 'watchdog interval'.

The WDT consists of an 8-bit timer (WDT) with a 9-bit prescaler. The prescaler is fed with 32 kHz which always runs, even if the 8051 is in SLEEP state. The 8 bit WDT timer is decremented every (1/32KHz) *512 seconds or 16.0 ms. Thus, the watchdog interval is programmable between 16ms and 4.08 seconds on 16ms intervals.

WDT ACTION

If the 8 bit timer (WDT) underflows, a VCC1 POR is generated

8051 in Idle Mode - WDT will be active if enabled. When the WDT timer underflows in idle mode, the 8051 will be reset. It is up to the firmware engineer to design code that uses a timer to generate an interrupt that will exit idle mode and re-initialize the WDT timer and then put the 8051 back into idle mode.

8051 in Sleep Mode - If enabled, the WDT is active since it is running off of the 32 KHz clock. Therefore, if the WDT is enabled the 8051 should never remain in the SLEEP state for more than 4 seconds.

WDT ACTIVATION

Upon VCC1 POR the Watch Dog Timer powers up inactive. The Watch Dog Timer is activated when the WDT enable bit (WDT CONTROL bit D1) is set by 8051 firmware. The WDT may be disabled under software control through a specific sequence. Software can clear the SDT enable bit by:
Setting the WLE-WDT Load enable bit in the WDT Control/Status Register.
Writing 00h to the WDT Timer Register (this causes the WDT Enable and the WLE_WDT Load Enable bits to each reset to 0).

Once the WDT has been activated, this sequence must be executed in order to disable watchdog operation via software control. Note: Since a VCC1 POR will reset the WDT enable bit, the WDT must be re-enabled after each occurrence.

WDT RESET MECHANISM

The watchdog timer (WDT) must be reloaded within periods that are shorter than the programmed watchdog interval; otherwise the WDT will underflow and a VCC1 POR will be generated. It is the responsibility of the user program to continually execute sections of code which reload the 8 bit timer (WDT).

The WDT is reloaded in two stages in order to prevent erroneous software from reloading the watchdog. First WDT CONTROL bit D0 (WLE-WDT Load Enable) must be set. Then the WDT may be loaded. When the WDT is loaded WLE is automatically reset. WDT can not be loaded when WLE is reset. Since the WDT timer is a down counter, a reload value of 01h results in the minimum WDT interval (16ms) and a reload value of 0FFh results in the maximum WDT interval (4.08 seconds). Loading 00h into the WDT disables the WDT and clears the WDT Enable bit. Note, the 9 bit prescaler is initialized whenever the WDT timer is loaded.

WDT MEMORY MAPPED REGISTERS

TABLE 118 - WDT

HOST ADDRESS	N/A
8051 ADDRESS	0x 7F38
POWER	VCC1
DEFAULT	0xFF

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SYSTEM R/W	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
BIT DEF	WDT Timer	WDT Timer	WDT Timer	WDT Timer	WDT Timer	WDT Timer	WDT Timer	WDT Timer

TABLE 119 - WDT CONTROL/STATUS

HOST ADDRESS	N/A
8051 ADDRESS	0x 7F37
POWER	VCC1
DEFAULT	0x00

	D7-D2	D1	D0
8051 R/W	R	R/W	R/W
SYSTEM R/W	N/A	N/A	N/A
BIT DEF	Reserved	WDT Enable	WLE-WDT Load Enable

WLE

Watchdog Load Enable bit must be set to enable writing to the WDT Timer register. This bit is automatically reset when the 8051 writes to the WDT register. If this bit is reset, writes to the WDT register are ignored.

WDT Enable

The WDT enable bit must be set by 8051 firmware to enable or start the Watch Dog Timer. A VCC1 POR or the above described software sequence will reset this bit.

SHARED FLASH INTERFACE

A 256KB Flash Device (i.e., 28F004) is recommended to store the program code for the 8051 (Keyboard BIOS+) and the system BIOS. The FLASH memory can be accessed from the system in blocks of 64KB or from the 8051 in blocks of 32KB. The procedure to access the FLASH memory is described in the Host Flash Access section.

FLASH INTERFACE DIAGRAM

Access to the Flash Memory is multiplexed inside of the FDC37N972. The host CPU only has access to the Flash when nRESET_OUT is not asserted and the 8051 STP_CLK bit-0 is set. Please refer to the timing section for details on this interface.

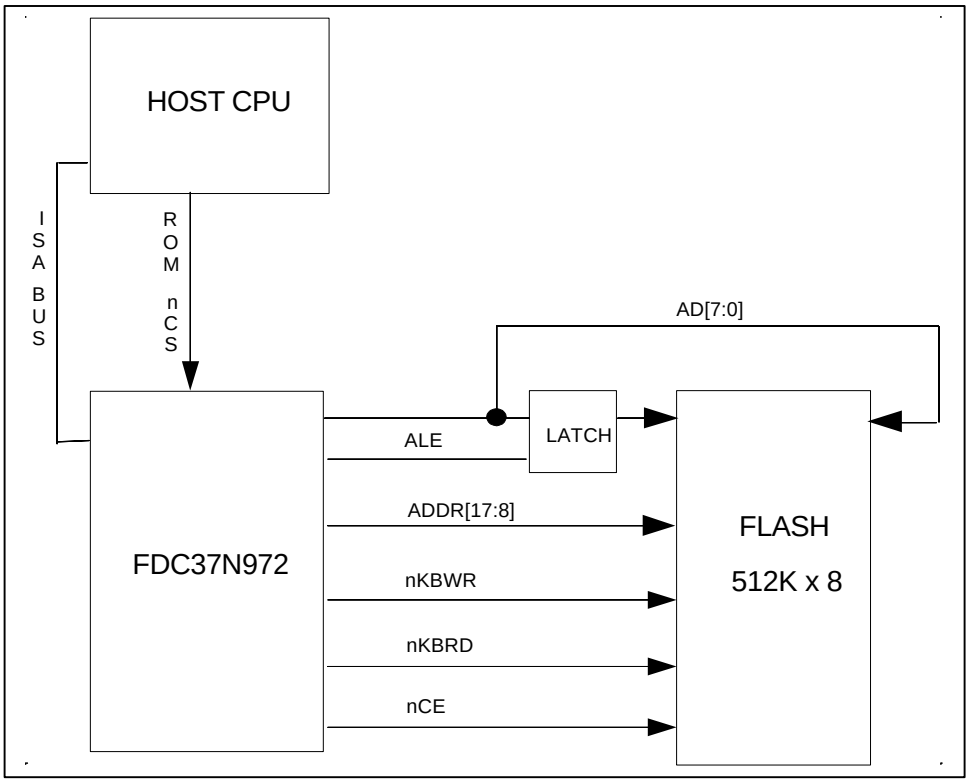


FIGURE 22 - FLASH INTERFACE DIAGRAM

SYSTEM MEMORY MAP

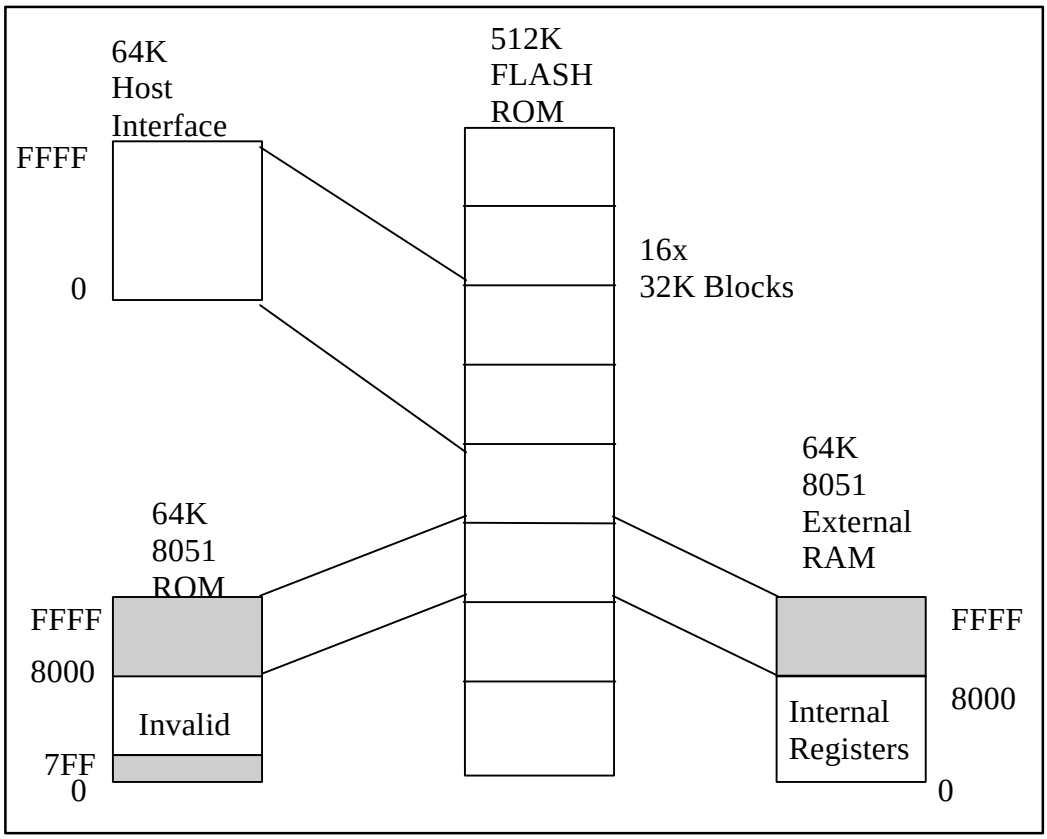


FIGURE 23 - SYSTEM FLASH ACCESS MAP (ALT BONDOUT)

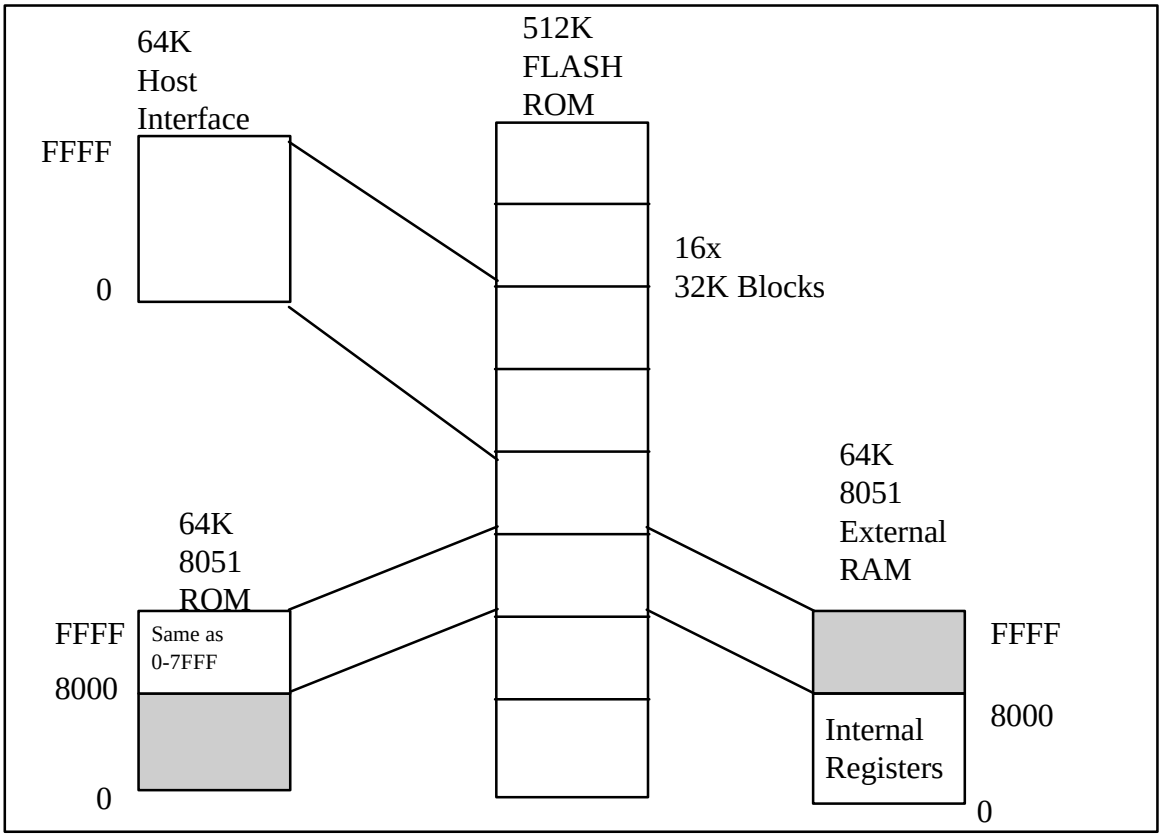


FIGURE 24 - SYSTEM FLASH ACCESS MAP (SMSC BONDOUT)

KEYBOARD BIOS (KMEM)

The 8051 uses this register to access the Flash ROM in a 32K window. The 8051 is only barred from accessing the Flash when 8051STP_CLK bit D0 =1 and nRESET_OUT= high or deasserted. Bit D3 is added to the KMEM Register to accommodate the high-order Flash ROM address bit FA18 (TABLE 120). The Flash ROM Memory Ranges are decoded as shown in TABLE 121.

TABLE 120 - KMEM REGISTER

HOST INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F29	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	RESERVED				A18	A17	A16	A15

KMEM			
17	16	15	Flash Memory Range
0	0	0	000- 7FFF
0	0	1	8000- FFFF
0	1	0	10000-17FFF
0	1	1	18000-1FFFF
1	0	0	20000-27FFF
1	0	1	28000-2FFFF
1	1	0	30000-37FFF
1	1	1	38000-3FFFF

TABLE 121 - FLASH ROM ADDRESS ENCODING

KMEM REGISTER ADDRESS RANGE SELECT BITS				DECODED FLASH ROM MEMORY RANGE
D3	D2	D1	D0	
0	0	0	0	00000 – 07FFF
0	0	0	1	08000 – 0FFFF
0	0	1	0	10000 – 17FFF
0	0	1	1	18000 – 1FFFF
0	1	0	0	20000 – 27FFF
0	1	0	1	28000 – 2FFFF
0	1	1	0	30000 – 37FFF
0	1	1	1	38000 – 3FFFF
1	0	0	0	40000 – 47FFF
1	0	0	1	48000 – 4FFFF
1	0	1	0	50000 – 57FFF
1	0	1	1	58000 – 5FFFF
1	1	0	0	60000 – 67FFF
1	1	0	1	68000 – 6FFFF
1	1	1	0	70000 – 77FFF
1	1	1	1	78000 – 7FFFF

SYSTEM BIOS (HMEM)

HMEM REGISTER

Host	MBX 0x95
8051	N/A
Power	VCC1
Default	VCC1 POR = 0x03 VCC2 POR = 0x03

The system uses this register to select a 64K window for access from the 256K Flash ROM. The host may access the Flash when RESET_OUT pin is de-asserted and 8051STP_CLK bit D0 = 1.

Bit D2 is added to the HMEM Register to accommodate the high-order Flash ROM address bit FA18 (TABLE 122).

TABLE 122 - HMEM REGISTER

HOST INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
MBX95h	-	VCC1	0x07 (VCC1 POR) 0x07 (VCC2 POR)

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**R**	**R**	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**
8051 TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
BIT NAME	RESERVED					A18	A17	A16

HOST FLASH ACCESS

The FDC37N972 has a special shared Flash ROM interface. The 8051 can be stopped to allow the Host CPU to access the flash ROM after a special handshake sequence is followed.

HOST INITIATED FLASH ACCESS

To access the FLASH memory, the 8051 must first be placed into idle mode, and then the 8051 clock must be stopped. Host flash reads and writes occur when the nROMCS pin is asserted along with nMEMRD or nMEMWR. The register bit “8051_STPCLK” needs to be set by the host to make the 8051 clock stop. The 8051 clock is only stopped when 8051STP_CLK=1 and when nRESET_OUT pin = high. Address bits A[15:0] are supplied by SA[15:0], address bits A[17:16] are supplied by configuration register HMEM. For Flash access, these address lines and bits are qualified (selected) by 8051STP_CLK=1, and the nRESET_OUT pin = high (nRESET_OUT is driven by the 8051). The 8051 STP_CLK is set to “1” and HMEM is set to 03h (effectively resulting in A[17:16] initializing as "11") whenever the 8051 clears the IRESET_OUT bit from “1” to “0”. This allows the system to execute from the upper 64K of the Flash memory at boot time. To access the other portions of the Flash memory, the system software must first change the values of HMEM[1:0] register to control address lines A[17:16]. The access to the Flash memory uses nFWR for a write and nFRD for a read.

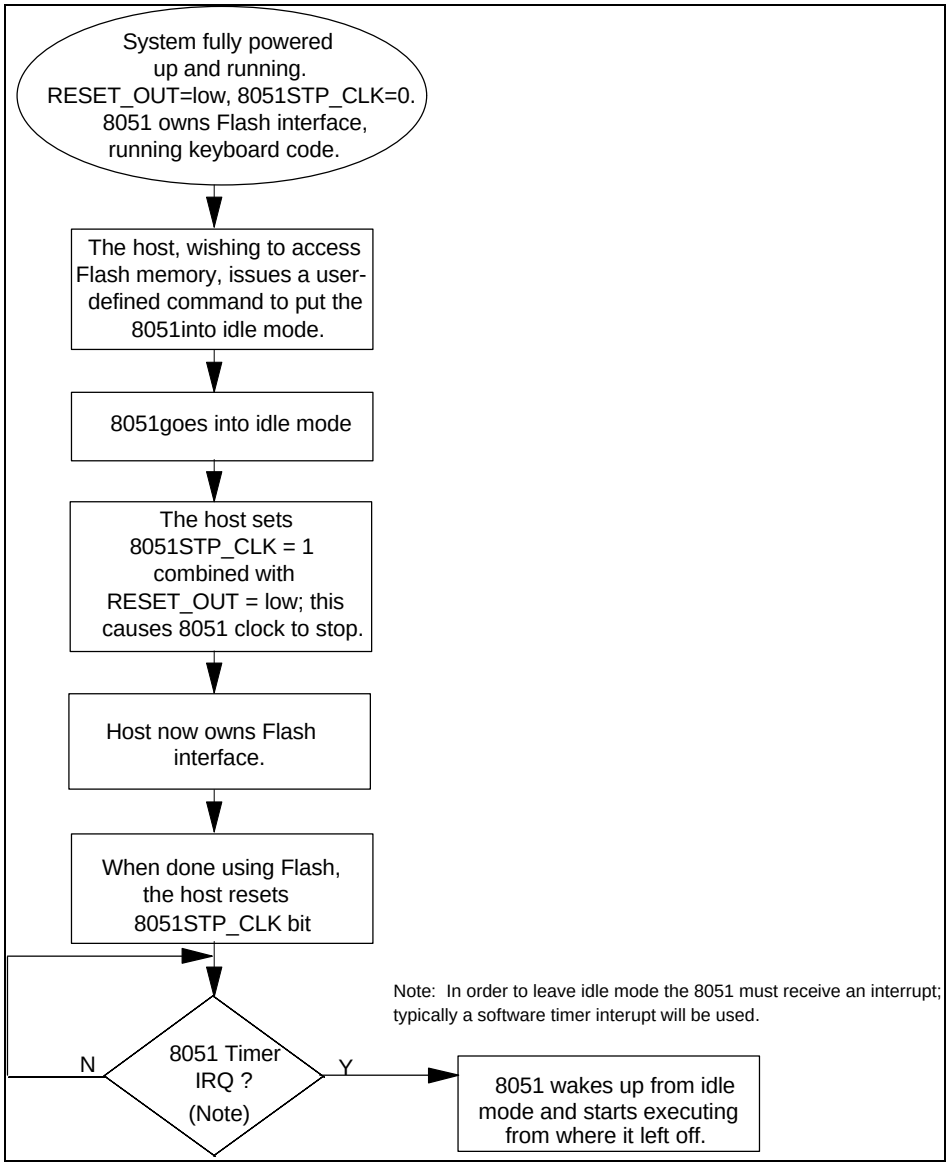


FIGURE 25 - DYNAMIC SHARING OF FLASH INTERFACE BETWEEN HOST AND 8051

TABLE 123 - 8051 STP_CLK REGISTER

Host	MBX 0x94
8051	N/A
Power	VCC1
Default	0x00

D7	D6	D5-D1	D0
IDLE	HOST_ FLASH	Reserved, set to “0”	0=8051 Clock can run 1=8051 Clock stop

Note: When bit D0=1 the 8051’s clock is not stopped unless the nRESET_OUT pin is also de-asserted at which point the host has access to the Flash Memory.
Note: Only bit D0 is R/W, bits[7:1] are Read only.

IDLE : 0 = 8051 not in idle mode
1= 8051 in idle mode

HOST_FLASH: 0 = Host does not have access to Flash, in use by 8051
1 = Host has access to Flash

HOST BOOT BLOCK SELECT

The FDC37N972 can optionally support 16k and 64k boot block Flash ROMs and can boot out of the same Flash ROM address space as the 8051.

The 64K HOST BOOT bit and the 16K HOST BOOT bit, D1 and D0 respectively in the Flash Configuration register (TABLE 127) determine the host boot block options (TABLE 124). For more information regarding the 64K HOST BOOT bit and the 16K HOST BOOT bit, see FLASH CONFIGURATION REGISTER on page 197.

The host boot block options described in TABLE 124 apply to host flash addresses, only.

TABLE 124 - HOST BOOT BLOCK OPTION

FLASH CONFIGURATION REGISTER		MODE	DESCRIPTION
D1	D0		
0	0	NORMAL	Host Flash Address Bits 18 – 16 are under control of the HMEM register (**default**).
0	1	16K MODE	Host Flash Address Bits 18 – 14 are forced to “0”.
1	0	64K MODE	Host Flash Address Bits 18 – 16 are forced to “0”.
1	1	UNDEFINED	**DO NOT USE.**

PROGRAMMABLE FLASH CHIP SELECT

The FDC37N972 Flash ROM Chip Select output nFCS can be optionally deasserted “1” when the 8051 is sleeping with control of the Flash, or asserted and deasserted according to the Flash ROM read strobe nFRD.

The ALT CHIP SELECT bit D2 in the Flash Configuration register (TABLE **127**) selects the Flash ROM Chip Select Option. The effects of the ALT CHIP SELECT bit are shown in TABLE 125. For more information regarding the ALT CHIP SELECT bit, see FLASH CONFIGURATION REGISTER on page 197.

TABLE 125 - FLASH ROM CHIP SELECT OPTIONS

FLASH CONFIG. REGISTER	MODE	DESCRIPTION
D2		
0	NORMAL	nFCS deasserted when 8051 is sleeping with control of the Flash (**default**).
1	READ	nFCS follows nFRD.

FLASH ROM WRITE REDIRECTION

The Flash ROM write control nFWR can be optionally redirected to an alternate function of the OUT3 pin to support functions like an I/O port expander.

The ALT WRITE SELECT bit D3 in the Flash Configuration register (TABLE **127**) selects the Flash ROM Write Redirection Option. The effects of the ALT WRITE SELECT bit are shown in **TABLE 126 - FLASH ROM WRITE REDIRECTION OPTIONS**.

For more information regarding the ALT WRITE SELECT bit, see FLASH CONFIGURATION REGISTER on page 197.

TABLE 126 - FLASH ROM WRITE REDIRECTION OPTIONS

FLASH CONFIG. REGISTER D3	MODE	DESCRIPTION
0	NORMAL	The OUT3 pin is configured as a General Purpose Output and Flash ROM "writes" appear on the nFWR pin (**default**).
1	WRITE REDIRECTION	The OUT3 pin is configured as an inverted Flash ROM "write" strobe, FWR. **NOTE:** Flash ROM "writes" do not appear on the nFWR pin but appear inverted on the FWR pin.

FLASH CONFIGURATION REGISTER

OVERVIEW

The Flash Configuration register (TABLE **127** is used to select the various options described in this document.)

The FCR is a VCC1 register. The bits in the FCR are R/W and cleared by VCC1 POR. Detailed descriptions of these bits follow, below.

TABLE 127 - FLASH CONFIGURATION REGISTER

HOST ADDRESS	-
8051 ADDRESS	0x7FFC
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	RESERVED				ALT WRITE SELECT	ALT CHIP SELECT	64K HOST BOOT[1]	16K HOST BOOT[1]

NOTE[1] Bits D0 and D1 are cleared by VCC1_POR or host writes to the HMEM register.

ALT WRITE SELECT Bit, D3

The ALT WRITE SELECT bit is used to select Flash ROM Write Redirection Option shown in **TABLE 126 - FLASH ROM WRITE REDIRECTION OPTIONS**.

See FLASH ROM WRITE REDIRECTION, above, for a description of this function. The ALT WRITE SELECT bit is also used as the OUT3 pin alternate function multiplex control (**TABLE 4**). The 8051 can read and write the ALT WRITE SELECT bit. The bit is "0" by default and is cleared by VCC1_POR.

ALT CHIP SELECT Bit, D2

The ALT CHIP SELECT bit selects the Flash ROM Chip Select Option shown in TABLE 125. See **PROGRAMMABLE FLASH CHIP SELECT**, above, for a description of this function. The 8051 can read and write the ALT CHIP SELECT bit. The bit is "0" by default and is cleared by VCC1_POR.

64K HOST BOOT Bit, D1

The 64K HOST BOOT bit is used to select the 64K MODE Host Boot Block option shown in **TABLE 124**. See HOST BOOT BLOCK SELECT, above, for a description of this function.

NOTE: The 16K HOST BOOT Bit D0 must not be set to a "1" when the 64K HOST BOOT bit is "1".

The 8051 can read and write the 64K HOST BOOT bit. The 64K HOST BOOT bit is cleared by VCC1_POR or host writes to the HMEM register.

16K HOST BOOT Bit, D0

The 16K HOST BOOT bit is used to select the 16K MODE Host Boot Block option shown in **TABLE 124**. See HOST BOOT BLOCK SELECT, above, for a description of this function.

NOTE: The 64K HOST BOOT Bit D1 must not be set to a "1" when the 16K HOST BOOT bit is "1".

The 8051 can read and write the 16K HOST BOOT bit. The 16K HOST BOOT bit is cleared by VCC1_POR or host writes to the HMEM register.

8051 SYSTEM POWER MANAGEMENT

The High-Performance 8051 core provides support for two further power-saving modes, available when inactive: Idle mode, typically entered between keystrokes; and sleep mode, entered upon command from the host. The High Performance 8051 is wakeable from sleep mode through a set of external and internal events called Wake-Up events. The events are listed in Table **128**. When exiting the Sleep mode, the High Performance 8051 will continue executing code from where it left off when put into sleep with no changes to the SFR and pins.

The FDC37N972 is fully static and will pickup from where it left off in the event of a wake-up event.

IDLE MODE

Entering IDLE mode:
Idle mode is initiated by an instruction that sets the PCON.0 bit (SFR address 87H) in the keyboard. In idle mode, the internal clock signal to the keyboard CPU is gated off, but not to the Interrupt Timer and Serial Port functions. The CPU status is preserved in its entirety: The Stack Pointer, Program Counter, Program Status Word, Accumulator, and all other registers maintain their data. The port pins hold the logical levels they had when Idle mode was activated.

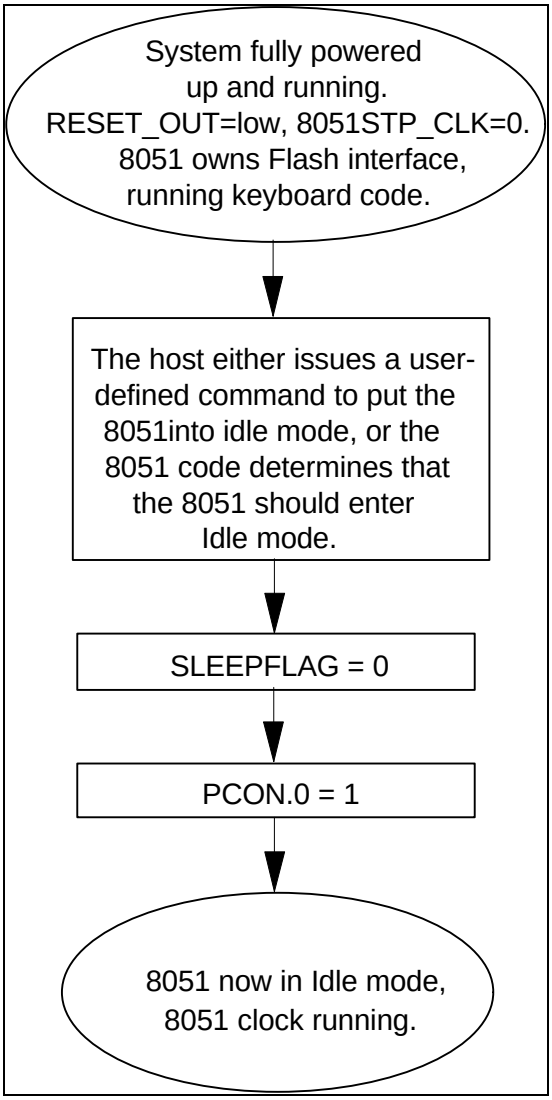


FIGURE 26 - ENTERING IDLE MODE

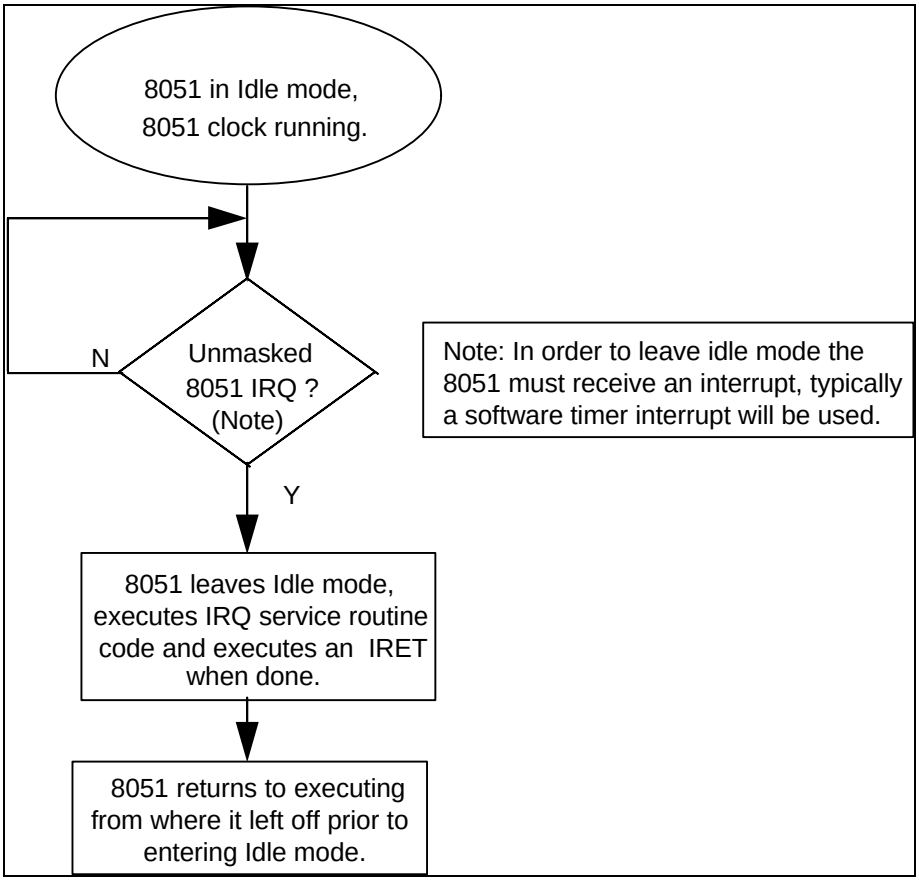


FIGURE 27 - EXITING IDLE MODE DUE TO IRQ

EXITING IDLE MODE

There are two ways to terminate Idle mode. First, activation of any enabled interrupt will cause the PCON.0 bit to be cleared by hardware. The interrupt will be serviced and, following the RETI, the CPU will resume operation by executing the instruction following the one that put the CPU into Idle mode.

The second way to terminate the Idle mode is with a VCC1 POR. Note that a VCC1 POR will clear the registers. The CPU will not resume program execution from where it left off.

SLEEP MODE

When the CPU enters sleep mode, all internal clocks, including the core clocks, are turned off. If an external crystal is used, the internal oscillator is turned off. RAM contents are preserved. Sleep mode is initiated by a user defined 8051 command sequence.

Sleep mode sequence
To enter sleep mode, the 8051:

turns on the ring oscillator (KSTP_CLK[4] = 1)
switches the clock source (KSTP_CLK[5] = 0)
turns off the clock chip (or the whole system power, VCC2) masks all interrupts except for INT5_h
sets SLEEPFLAG = 1
sets PCON.0 = 1
The ring oscillator will be automatically turned off
The 8051 goes into Sleep mode.

In sleep mode, the FDC, UART and parallel port are powered off if VCC2 is removed, but the RTC and 8051 are in powerdown (sleep) mode. In Sleep mode the FDC37N972 consumes less than 20μA, and all wake-up pins are still active.

When the 8051 is in sleep mode, all of the clocks are stopped and the 8051 is waiting for an unmasked wake-up event. When the wake-up event occurs, the ring oscillator is started the 8051 starts executing from where it stopped in the sleep Mode Sequence. Once running, the 8051 can access all of the registers that are on VCC1 and if VCC2 is at 3.3V it can access all of the registers on VCC2. The 8051 running from the ring oscillator (internal) clock source switch to an external clock sourceand then turn off the ring oscillator (internal) clock source.

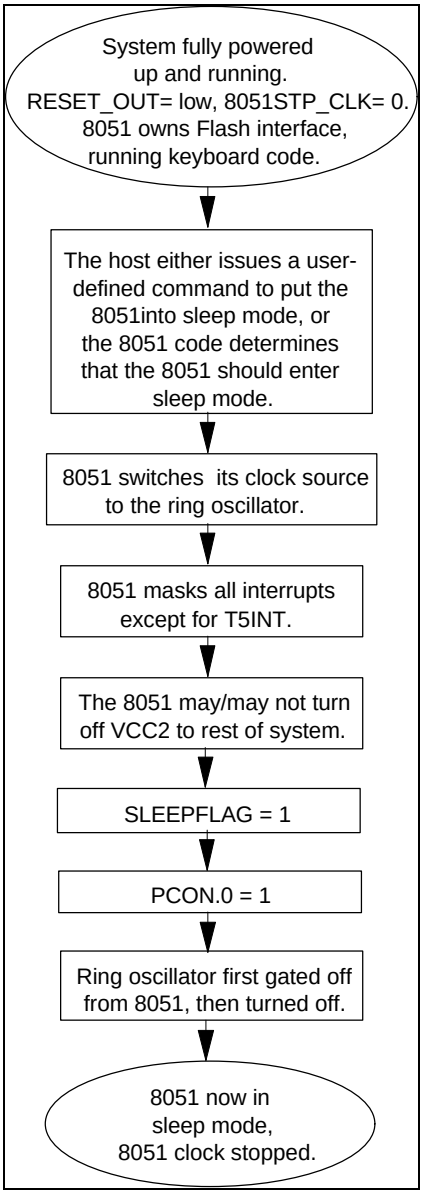


FIGURE 28 - ENTERING SLEEP MODE

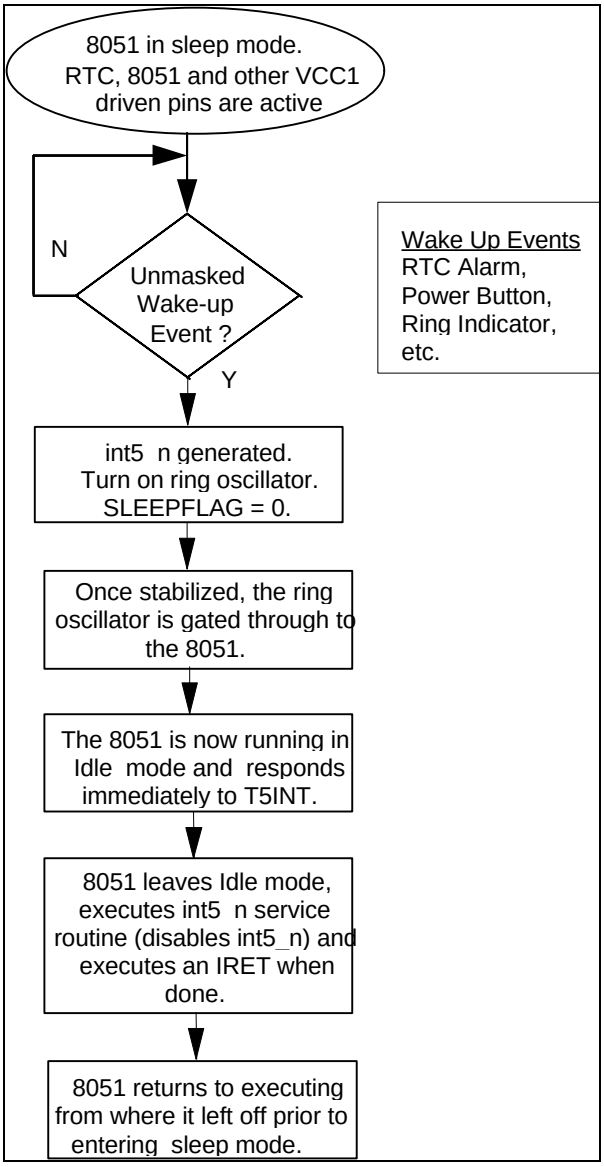


FIGURE 29 - EXITING SLEEP MODE

WAKE-UP EVENTS

There are two types of wake-up events that can occur, internal (TABLE 128 – INTERNAL SYSTEM WAKE-UP EVENTS) and external (TABLE 129). Wake-up events on General Purpose Pins can be either edge or selectable edges. Refer to table TABLE 109 for further description. Wake-up events can occur when VCC2 is off. VCC1 must be on for a wake-up event to occur, but the high-performance 8051 can be in sleep mode.

TABLE 128 – INTERNAL SYSTEM WAKE-UP EVENTS

WAKE-UP EVENTS	REGISTER	DESCRIPTION
RTC_ALRM	Wake Up Src 1 (0x7F2B) [D0]	RTC Alarm
HTIMER	Wake Up Src 2 (0x7F2B) [D2]	Hibernation Timer
PM1_STS2	Wake Up Src 1 (0x7F2A) [D5]	PM1 Status
PM1_EN2	Wake Up Src 1 (0x7F2A) [D6]	PM1 Enable
PM1_CTL2	Wake Up Src 1 (0x7F2A) [D7]	PM1 Control

TABLE 129 - EXTERNAL SYSTEM WAKE-UP EVENTS

PIN	WAKE-UP EVENTS	ACTIVE EDGE	REGISTER	DESCRIPTION
nRI	UART_RI1	Edge, high-to-low	Wake Up Src 2 (0x7F2B) [D6]	UART Ring Indicator
AB1_DATA	ACCBUS1	Leading edge, high-to-low	Wake Up Src1 (0x7F2A) [D4]	AB_DAT ACCESS BUS1
AB2_DATA	ACCBUS2	Leading edge, high-to-low	Wake Up Src1 (0x7F2A) [D3]	AB_DAT ACCESS BUS2
IRRX	IR_RX	Edge, high-to-low	Wake Up Src1 (0x7F2B) [D2]	IR energy detected on the IRRX Receive pin
KSI[7:0]	WK_ANYKEY	Edge, high-to-low	Wake Up Src 2 (0x7F2B) [D1]	Any Keyboard Key pressed
GPIO0/	WK_SE02	PROGRAMMABLE	Wake Up Src 4 (0x7F59) [D2]	General Purpose Pin
GPIO1	WK_SE03	PROGRAMMABLE	Wake Up Src 4 (0x7F59) [D3]	General Purpose Pin
GPIO2	WK_SE04	PROGRAMMABLE	Wake Up Src 4 (0x7F59) [D4]	General Purpose Pin
GPIO3	TRIGGER	PROGRAMMABLE	INT SRC 1 (0x7F02) [D3]	General Purpose Pin
GPIO4	WK_SE07	PROGRAMMABLE	Wake Up Src 4 (0x7F59) [D7]	General Purpose Pin

PIN	WAKE-UP EVENTS	ACTIVE EDGE	REGISTER	DESCRIPTION
GPIO5	WK_SE10	PROGRAMMABLE	Wake Up Src 5 (0x7F5E) [D0]	General Purpose Pin
GPIO6	WK_SE11	PROGRAMMABLE	Wake Up Src 5 (0x7F5E) [D1]	General Purpose Pin Or FIR Mode Output/ 2nd Receive Input
GPIO7	WK_SE06	PROGRAMMABLE	Wake Up Src 4 (0x7F59) [D6]	General Purpose Pin
GPIO8	WK_SE12	PROGRAMMABLE	Wake Up Src 5 (0x7F5E) [D2]	GPIO8 or IR energy detected on the GPIO/COM-RX Receive pin.
GPIO9	WK_SE13	PROGRAMMABLE	Wake Up Src 5 (0x7F5E) [D3]	General Purpose Pin
GPIO10	WK_SE14	PROGRAMMABLE	Wake Up Src 5 (0x7F5E) [D4]	General Purpose Pin Or FIR Mode Output/ 2nd Receive Input
GPIO11	WK_SE15	PROGRAMMABLE	Wake Up Src5 (0x7F5E) [D5]	GPIO11 or ACCESS.bus 2 Serial Data
GPIO12	WK_SE16	PROGRAMMABLE	Wake Up Src5 (0x7F5E) [D6]	GPIO12 or ACCESS.bus 2 Clock
GPIO13	WK_SE17	PROGRAMMABLE	Wake Up Src5 (0x7F5E) [D7]	General Purpose Pin
GPIO14	WK_SE20	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D0]	General Purpose Pin
GPIO15	WK_SE21	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D1]	General Purpose Pin
GPIO16	WK_SE22	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D2]	General Purpose Pin
GPIO17	WK_SE23	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D3]	General Purpose Pin
GPIO18	WK_SE27	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D7]	GPIO18 or DMA Acknowledge
GPIO19	WK_SE24	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D4]	General Purpose Pin /DMA Acknowledge
GPIO20/ PS2CLK/ 8051RX	WK_SE25	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D5]	General Purpose Pin /PS2 Serial Clock 8051 RX Input
GPIO21/ PS2DAT/ 8051TX	WK_SE26	PROGRAMMABLE	Wake Up Src6 (0x7F63) [D6]	General Purpose Pin /PS2 Serial Data 8051 TX Input
IN0	WK_EE4	Either Edge	Wake Up Src 2 (0x7F2B) [D5]	General Purpose Wakeup Source

PIN	WAKE-UP EVENTS	ACTIVE EDGE	REGISTER	DESCRIPTION
IN1	WK_EE2	Either Edge	Wake Up Src 2 (0x7F2B) [D4]	General Purpose Wakeup Source
IN2	WK_EE3	Either Edge	Wake Up Src 2 (0x7F2B) [D5]	General Purpose Wakeup Source
IN3	nGPWKUP	Either Edge	Wake Up Src 2 (0x7F2B) [D3]	General Purpose Wakeup Source
IN4	WK_SE00	Either Edge	Wake Up Src 4 (0x7F59) [D0]	General Purpose Wakeup Source
IN5	WK_SE01	Either Edge	Wake Up Src 4 (0x7F59) [D1]	General Purpose Wakeup Source
IN6	WK_SE05	Either Edge	Wake Up Src 4 (0x7F59) [D5]	General Purpose Wakeup Source
IN7	WK_EE1	Either Edge	Wake Up Src1 (0x7F2B) [D1]	General Purpose Wakeup Source

NOTE: All GPIO pins can generate wake events and all alternate functions of GPIO primary function pins can generate wake events.

KEYBOARD CONTROLLER

8042 STYLE HOST INTERFACE

The FDC37N972 keyboard controller uses a High-Performance 8051 microcontroller CPU core to produce a superset of the features provided by the industry-standard 8042 keyboard controller. Added features include two high-drive serial interfaces, and additional interrupt sources. The FDC37N972 provides an industry standard 8042-style host interface to the High-Performance 8051 to emulate standard 8042 keyboard controller and preserve software backward compatibility with the system BIOS. The FDC37N972's keyboard ISA interface is functionally compatible with the 8042-style host interface. It consists of the SD[0:7] data bus; the nIOR, nIOW and the KBD (Keyboard) Status register, KBD Data/Command Write register, and KBD Data Read register. Table 130 shows how the interface decodes the control signals. In addition to the above signals, the host interface includes keyboard and mouse IRQ's.

TABLE 130 - KEYBOARD CONTROLLER ISA I/O ADDRESS MAP

ISA ADDRESS	NIOW	NIOR	FUNCTION (NOTE 1, 2)
0x60	0	1	Keyboard Data Write (C/D=0)
	1	0	Keyboard Data Read
0x64	0	1	Keyboard Command Write (C/D=1)
	1	0	Keyboard Status Read

All addresses are qualified by AEN.

Note 1: The Keyboard Interface can be enabled or disabled through the configuration registers.
Note 2: These registers consist of three separate 8 bit registers: KBD Status, KBD Data/Command Write and KBD Data Read.

KEYBOARD DATA WRITE

This is an 8 bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

KEYBOARD DATA READ

This is an 8 bit read only register. When read, the PBOBF and/or AUXOBF interrupts are cleared and the OBF flag in the status register is cleared.

KEYBOARD COMMAND WRITE

This is an 8 bit write only register. When written, the C/D status bit of the status register is set to one and the IBF bit is set.

KEYBOARD STATUS READ

This is an 8 bit read only register. Refer to the description of the Status Register (7FF2H) for more information.

8051- TO- HOST KEYBOARD COMMUNICATION

The 8051 can write to the KBD Data Read register via address 7FF1H and 7FFAH (Aux Host Data Register) respectively. A write to either of these addresses automatically sets bit 0 (OBF) in the Status register. A write to 7FF1H also sets PCOBF. A write to 7FFAH also sets AUXOBF1. See TABLE 132 below.

TABLE 131 - HOST-INTERFACE FLAGS

8051 ADDRESS	FLAG
7FF1H (R/W)	PCOBF (KIRQ) output signal goes high
7FFAH (W)	AUXOBF1 (MIRQ) output signal goes high

HOST I/F DATA REGISTER

Host	ISA 0x60
8051	0x7FF1
Power	VCC1
Default	N/A

The Input Data register and Output Data register are each 8 bits wide. A write to this 8 bit register by the 8051 will load the Keyboard Data Read Buffer, set the OBF flag and set the PCOBF output if enabled. A read of this register by the 8051 will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag. Refer to the PCOBF and Status register descriptions for more information.

HOST I/F COMMAND REGISTER

Host	ISA 0x64 (W)
8051	0x7FF1
Power	VCC1
Default	N/A

The host CPU sends commands to the keyboard controller by writing command bytes to ISA port 0x64.

HOST I/F STATUS REGISTER

Host	ISA 0x64 (R)
8051	0x7FF2
Power	VCC1
Default	N/A

The Status register is 8 bits wide. Shows the contents of the KBD Status register.

TABLE 132 - KBD STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
UD	UD	AUXOBF/UD	UD	C/D	UD	IBF	OBF

This register is read-only for the Host and read/write by the 8051. The 8051 cannot write to bits 0, 1, or 3 of the Status register.

UD Read/Writeable by 8051. These bits are user-definable.

C/D

Command Data - This bit specifies whether the input data register contains data or a command (“0” = data, “1” = command). During a host data/command write operation, this bit is set to "1" if SA2 = “1” or reset to "0" if SA2 = 0.

IBF

Input Buffer Full - This flag is set to “1” whenever the host system writes data into the input data register. Setting this flag activates the 8051's nIBF interrupt if enabled. When the 8051 reads the input data register, this bit is automatically reset and the interrupt is cleared. There is no output pin associated with this internal signal.

OBF

Output Buffer Full - This flag is set to “1” whenever the 8051 writes into the data registers at 7FF1H or 7FFAH. When the host system reads the output data register, this bit is automatically reset.

AUXOBF

Auxiliary Output Buffer Full - This flag is set to “1” whenever the 8051 writes into the data registers at 7FFAH. This flag is reset to “0” whenever the 8051 writes into the data registers at 7FF1H.

PCOBF

Host	N/A
8051	0x7FFD
Power	VCC1
Default	0x00

Refer to the PCOBF description for information on this register. This is a “1” bit register (bits 1-7=0 on read)

HOST-TO 8051 KEYBOARD COMMUNICATION

The host system can send both commands and data to the KBD Data/Command Write register. The CPU differentiates between commands and data by reading the value of bit 3 of the Status register. When bit 3 is "1", the CPU interprets the register contents as a command. When Bit 3 is "0", the CPU interprets the register contents as data. During a host write operation, bit 3 is set to "1" if SA2 = 1 or reset to "0" if SA2 = 0.

PCOBF DESCRIPTION

(The following description assumes that OBFEN = 1 in Configuration Register 0); PCOBF is gated onto KIRQ. The KIRQ signal is a system interrupt which signifies that the 8051 has written to the KBD Data Read register via address 7FF1H. On power-up, PCOBF is reset to 0. PCOBF will normally reflect the status of writes to 7FF1H, if PCOBFEN (bit 2 of Configuration register “0”) = “0”. (KIRQ is normally selected as IRQ1 for keyboard

support.) PCOBF is cleared by hardware on a read of the Host Data Register.

Additional flexibility has been added which allows firmware to directly control the PCOBF output signal, independent of data transfers to the host-interface data output register. This feature allows the FDC37N972 to be operated via the host "polled" mode. This firmware control is active when PCOBFEN = 1 and firmware can then bring PCOBF high by writing a "1" to the LSB of the 1 bit data register, PCOBF, allocated at 7FFDH. The firmware must also clear this bit by writing a "0" to the LSB of the 1 bit data register at 7FFDH.

The PCOBF register is also readable; bits 1-7 will return a "0" on the read back. The value read back on bit 0 of the register always reflects the present value of the PCOBF output. If PCOBFEN = 1, then this value reflects the output of the firmware latch at 7FFDH. If PCOBFEN = 0, then the value read back reflects the in-process status of write cycles to 7FF1H (i.e., if the value read back is high, the host interface output data register has just been written to). If OBFEN=0, then KIRQ is driven inactive (low).

AUXOBF1 DESCRIPTION

(The following description assumes that OBFEN = 1 in Configuration Register 0); This bit is multiplexed onto MIRQ. The AUXOBF1/MIRQ signal is a system interrupt which signifies that the 8051 has written to the output data register via address 7FFAH.

On power-up, after VCC1 POR, AUXOBF1 is reset to 0. AUXOBF1 will normally reflects the status of writes to 7FFAH. (MIRQ is normally selected as IRQ12 for mouse support.) AUXOBF1 is cleared by hardware on a read of the Host Data Register. If OBFEN=0, then KIRQ is driven inactive (low).

	HOST I/F STATUS REGISTER BITS			
Write to Register	AUXOBF (D5)	OBF (D0)	OBFEN=0	OBFEN=1
7FF1	0	1	KIRQ=0	KIRQ=1
7FFA	1	1	MIRQ=0	MIRQ=1

OBFEN	**PCOBFEN**	
0	X	KIRQ is inactive and driven low
1	0	KIRQ = PCOBF@7FF1
1	1	KIRQ = PCOBF@7FFD

OBFEN	**AUXH**	
0	X	MIRQ is inactive and driven low
1	0	MIRQ = PCOBF@7FFA; Status Register D5 = User Defined
1	1	MIRQ = PCOBF@7FFA; Status Register D5 = Hardware Controlled

8051 AUXOBF1 CONTROL REGISTER
AUX HOST DATA REGISTER

Host	ISA 0x60
8051	0x7FFA
Power	VCC1
Default	N/A

Refer to the AUXOBF1 description for information on this register.

GATEA20 HARDWARE SPEED-UP

GATEA20 is multiplexed onto GPIO17 using MISC6. The FDC37N972 contains on-chip logic support for the GATEA20 hardware speed-up feature. GATEA20 is part of the control required to mask address line A20 to emulate 8086 addressing.

In addition to the ability for the host to control the GATEA20 output signal directly, a configuration bit called "SAEN" (Software Assist Enable, bit 1 of Configuration register 0) is provided; when set, SAEN allows firmware to control the GATEA20 output.

When SAEN is set, a 1 bit register assigned to address 7FFBH controls the GATEA20 output. The register bit allocation is shown in Table 133.

TABLE 133 - REGISTER BIT ALLOCATION

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	x	GATEA20

Writing a "0" into location D0 causes the GATEA20 output to go low, and vice versa. When the register at location 7FFBH is read, all unused bits (D7-D1) are read back as "0".

Host control and firmware control of GATEA20 affect two separate register elements. Read back of GATEA20 through the use of 7FFBH reflects the present state of the GATEA20 output signal: if SAEN is set, the value read back corresponds to the last firmware-initiated control of GATEA20; if SAEN is reset, the value read back corresponds to the last host-initiated control of GATEA20.

Host control of the GATEA20 output is provided by the hardware interpretation of the "GATEA20 sequence" (see **TABLE 134**). The foregoing description assumes that the SAEN configuration bit is reset.

When the FDC37N972 receives a "D1" command followed by data (via the host interface), the on-chip hardware copies the value of data bit 1 in the received data field to the GATEA20 host latch. At no time during this host-interface transaction will PCOBF or the IBF flag (bit 1) in the Status register be activated; i.e., this host control of GATEA20 is transparent to firmware, with no consequent degradation of overall system performance. Table 134 details the possible GATEA20 sequences and the FDC37N972 responses.

On VCC1 POR, GATEA20 will be set.

An additional level of control flexibility is offered via a memory-mapped synchronous set and reset capability. Any data written to 7FFEH causes the GATEA20 host latch to be set; any

data written to 7FFFH causes it to be reset. This control mechanism should be used with caution. It was added to augment the "normal" control flow as described above, not to replace it. Since the host and the firmware have asynchronous control capability of the host latch via this mechanism, a potential conflict could arise. Therefore, after using the 7FFEH and 7FFFH addresses, firmware should read back the GATEA20 status via 7FFBH (with SAEN = 0) to confirm the actual GATEA20 response.

TABLE 134 - GATE20 COMMAND/DATA SEQUENCE EXAMPLES

SA2	R/W	D[0:7]	IBF	GATEA20	COMMENTS
1	W	D1	0	Q	GATEA20 Turn-on Sequence
0	W	DF	0	1	
1	W	FF	0	1	
1	W	D1	0	Q	GATEA20 Turn-off Sequence
0	W	DD	0	0	
1	W	FF	0	0	
1	W	D1	0	Q	GATEA20 Turn-on Sequence(*)
1	W	D1	0	Q	
0	W	DF	0	1	
1	W	FF	0	1	
SA2	**R/W**	**D[0:7]**	**IBF**	**GATEA20**	**COMMENTS**
1	W	D1	0	Q	GATEA20 Turn-off Sequence(*)
1	W	D1	0	Q	
0	W	DD	0	0	
1	W	FF	0	0	
1	W	D1	0	Q	Invalid Sequence
1	W	XX**	1	Q	
1	W	FF	1	Q	

Notes:
All examples assume that the SAEN configuration bit is 0.
"Q" indicates the bit remains set at the previous state.
*Not a standard sequence.
**XX = Anything except D1.
If multiple data bytes, set IBF and wait at state 0. Let the software know something unusual happened.
For data bytes SA2=0, only D[1] is used; all other bits are don't care.

8051 GATEA20 CONTROL REGISTERS

GATEA20

Host	N/A
8051	0x7FFB
Power	VCC1
Default	0x01

Refer to the GATEA20 Hardware Speed-up description for information on this register. This is a one bit register (Bits 1-7=0 on read)

SETGA20L

Host	N/A
8051	0x7FFE (W)
Power	VCC1
Default	N/A

Refer to the GATEA20 Hardware Speed-up description for information on this register. A write to this register sets GateA20.

RSTGA20L

Host	N/A
8051	0x7FFF (W)
Power	VCC1
Default	N/A

Refer to the GATEA20 Hardware Speed-up description for information on this register. A write to this register re-sets GateA20.

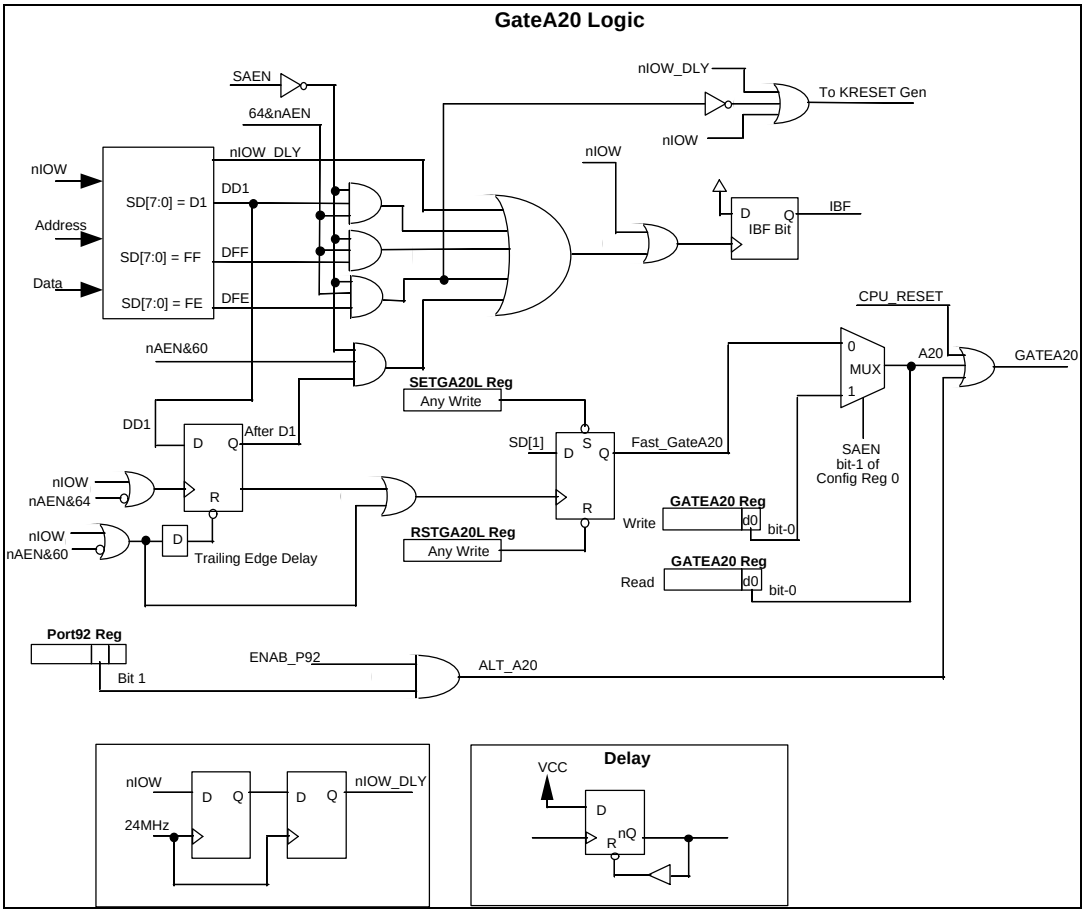


FIGURE 30 - GATEA20 IMPLEMENTATION DIAGRAM

CPU_RESET HARDWARE SPEED-UP

The ALT_CPU_RESET bit generates, under program control, the nALT_RST signal, which provides an alternate, means to drive the FDC37N972 CPU_RESET pin which in turn is used to reset the Host CPU. The nALT_RST signal is internally NANDed together with the nKBDRESET pulse from the KRESET Speed up logic to provide an alternate software means of resetting the host CPU. Note: before another nALT_RST pulse can be generated, ALT_CPU_RESET must be cleared to "0" either by a system reset (nRESET_OUT asserted) or by a write to the Port92 register with bit 0 = "0". A nALT_RST pulse is not generated in the event that the ALT_CPU_RESET bit is cleared and set before the prior nALT_RESET pulse has completed.

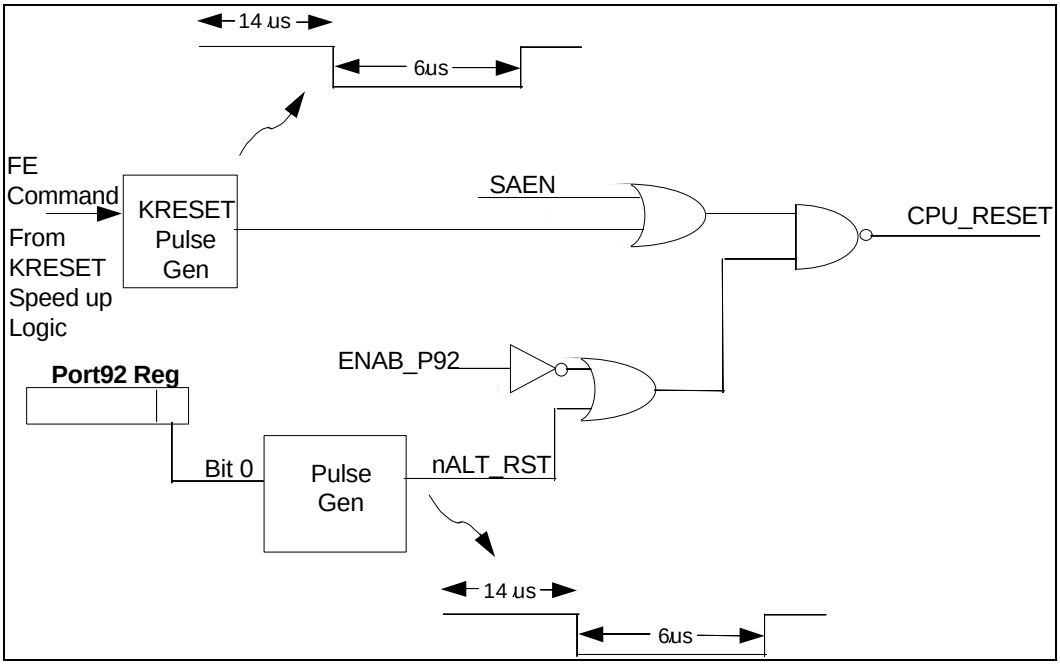


FIGURE 31 - CPU_RESET IMPLEMENTATION DIAGRAM

PORT 92

The FDC37N972 supports ISA I/O writes to port 92h as a quick alternate mechanism for generating a CPU_RESET pulse or controlling the state of GATEA20.

PORT 92 REGISTER DESCRIPTION

	D7-D2	D1	D0
Host R/W	R/W	R/W	R/W
Bit Def	0 Reserved	ALT_GATEA20	ALT_CPU_RESET

The Port92h register resides at ISA address 0x92 and is used to support the alternate reset (nALT_RST) and alternate GATEA20 (ALT_A20) functions. This register defaults to 0x00 on assertion of nRESET_OUT or on VCC2 Power On Reset.

Setting the Port 92 Enable bit (bit 0 of Logical Device 7 Configuration Register 0xF0) enables the Port92h Register. When Port92 is disabled, by clearing the Port 92 Enable bit, then access to this register is completely disabled (I/O writes to ISA 92h are ignored and I/O reads float the system data bus SD[7:0]).

When Port92h is enabled the bits have the following meaning:

D7-D2 RESERVED

A write are ignored and a read return 0.

D1 - ALT_GATEA20

This bit provides an alternate means for system control of the FDC37N972 GATEA20 pin.

= 0: ALT_A20 is driven low
= 1: ALT_A20 is driven high

When Port 92 is enabled, writing a 0 to bit 1 of the Port92 Register forces ALT_A20 low. ALT_A20 low drivesGATEA20 low, if A20 from the keyboard controller is also low. When Port 92 is enabled, writing a 1 to bit 1 of the Port92 register forces ALT_A20 high. ALT_A20 high drives GATEA20 high regardless of the state of A20 from the keyboard controller.

D0 - ALT_CPU_RESET

This bit provides an alternate means to generate a CPU_RESET pulse. The CPU_RESET output provides a means to reset the system CPU to effect a mode switch from Protected Virtual Address Mode to the Real Address Mode. This provides a faster means of reset than is provided through the 8051 keyboard controller. Writing a “1” to this bit will cause the nALT_RST internal signal to pulse (active low) for a minimum of 6µs after a delay of 14µs. Before another nALT_RST pulse can be generated, this bit must be written back to “0”.

The hardware GATEA20 state machine returns to state S1 from state S2 when CMD = D1 (FIGURE 32).

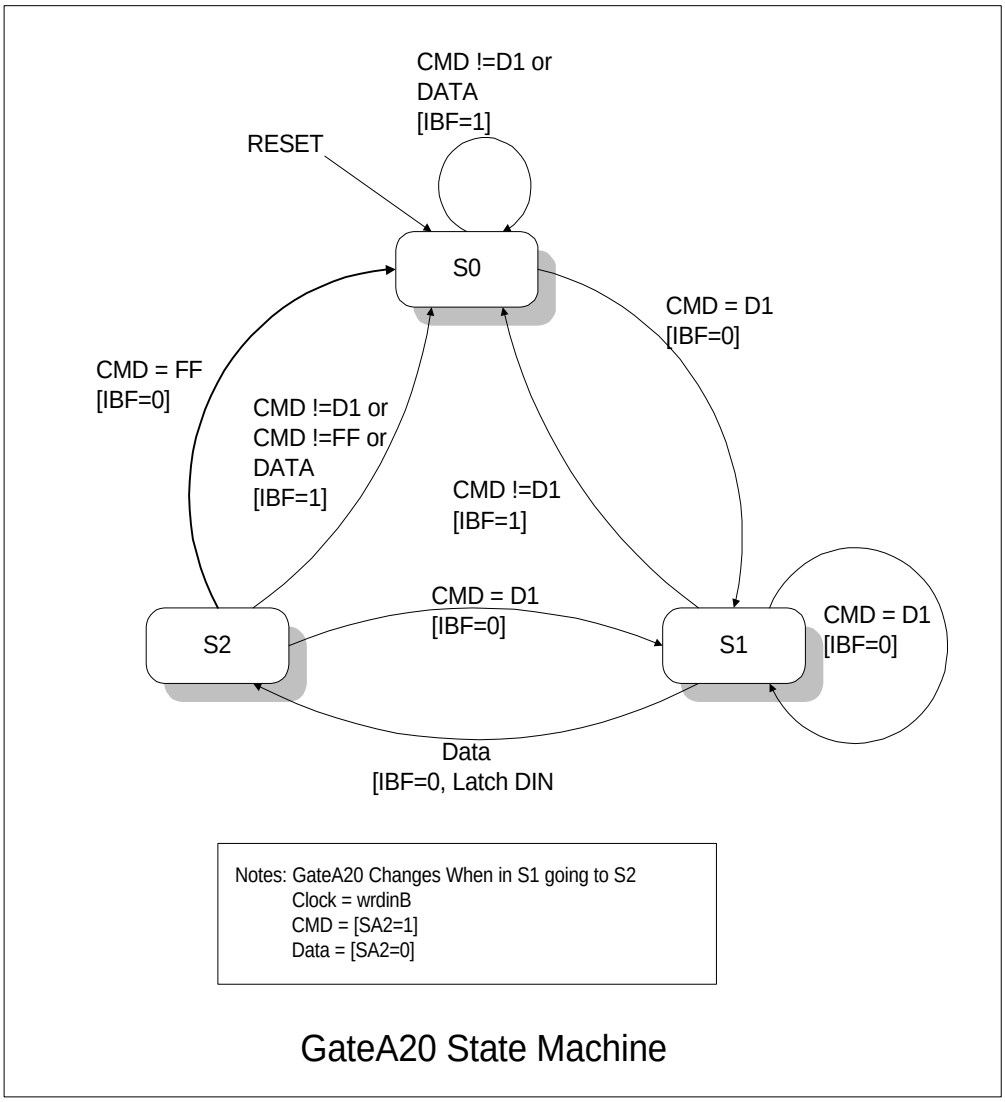


FIGURE 32 - GATEA20 STATE MACHINE

DIRECT KEYBOARD SCAN

The FDC37N972 scanning keyboard controller is designed for intelligent keyboard management in computer applications. By properly configuring GPIO4 and GPIO5, the FDC37N972 may be programmed to directly control keyboard interface matrixes of up to 16x8.

KEYBOARD SCAN-OUT REGISTER

Host	N/A
8051	0x7F04 (W)
Power	VCC1
Default	0x20

	D7-D6	D5	D4	D3	D2	D1	D0
8051 R/W	W	W	W	W	W	W	W
Bit Def	N/A	KSEN	1 = forces all KSO lines to go low	D5 and D4 must be '0' D[3:0] = 0000 KSO[0] is asserted low D[3:0] = 0001 KSO[1] is asserted low D[3:0] = 0010 KSO[2] is asserted low D[3:0] = 0011 KSO[3] is asserted low • • • D[3:0] = 1101 KSO[13] is asserted low D[3:0] = 1110 KSO[14] is asserted low D[3:0] = 1111 KSO[15] is asserted low			

KSEN 1 = disable scanning of internal keyboard (all the KSOUT lines going high) (D4-D0 are don't cares)
0 = enable scanning of internal keyboard
Note: Setting D[3:0] to 111x puts KSO0 - KSO13 outputs as Hi-Z.

KEYBOARD SCAN-IN REGISTER

Host	N/A
8051	0x7F04 (R)
Power	VCC1
Default	N/A

	D7-D0
8051 R	R
Bit description	Reflects the state of KSI [7:0]

The value of the KSI[x] pins can be read through this register.
The pin values are latched during the read.

EXTERNAL KEYBOARD AND MOUSE INTERFACE

Industry-standard PC/AT-compatible keyboards employ a two-wire, bidirectional TTL interface for data transmission. Several sources also supply PS/2 mouse products that employ the same type of interface. To facilitate system expansion, the FDC37N972 provides four pairs of signal pins that may be used to implement this interface directly for an external keyboard and mouse.

The FDC37N972 has four high-drive, open-drain output (external pull-ups are required), bidirectional port pins that can be used for external serial interfaces, such as ISA external keyboard and PS/2-type mouse interfaces. They are KBCLK, KBDAT, EMCLK, EMDAT, IMCLK, IMDAT, PS2CLK and PS2DAT.

The following function is assumed to be in the PS/2 PORT logic: The serial clock lines, KBCLK, EMCLK, IMCLK and PS2CLK, are cleared to a low by VCC2 POR. This is so that any power-on self-test completion code transmitted from the serial keyboard will not be missed by the FDC37N972 due to power-up timing mismatches.

PS/2 DEVICE INTERFACE

The FDC37N972 has four independent PS/2 serial ports implemented in hardware which are directly controlled by the on chip 8051. The hardware implementation eliminates the need to bit bang I/O ports to generate PS/2 traffic, however bit banging is still available if required.

Each of the four PS/2 serial channels use a synchronous serial protocol to communicate with the auxiliary device. Each PS/2 channel has two signal lines: Clock and Data. Both signal lines are bi-directional and employ open drain outputs capable of sinking 16mA. A pull-up resistor (typically 10K) is connected to the clock and data lines. This allows either the FDC37N972 SMSC PS/2 logic or the auxiliary device to control both lines. Regardless, the auxiliary device provides the clock for transmit and receive operations. The serial packet is made up of eleven bits, listed in order as they will appear on the data line: start bit, eight data bits (least significant bit first), odd parity, and stop bit. Each bit cell is from 60µS to 100µS long.

The SMSC PS/2 and the Devil Logic interfaces are available in the FDC37N972. The PS2_SEL Control bit D4 in Configuration Register 0 (0x7FF4) is used select between these two mutually exclusive options. (See **TABLE 90 - CONFIGURATION REGISTER 0**.) Many of the SMSC PS/2 and the Devil Logic registers share the same address space in the 8051 MMCRs. These are shown in TABLE 86 between addresses 0x7F41 and 0x7F4F.

See 8051 INT0 Source REGISTER on page 172 for a description of the Devil Logic versus the SMSC PS/2 interrupts and a description of the repsective pin mapping.

TABLE 135 - PIN DEFINITIONS

PIN NUMBER	PIN NAME	SMSC PS/2 FUNCTION	SMSC PS/2 DESCRIPTION
45	GPIO20	PS2CLK	Channel D Serial Clock
46	GPIO[21]	PS2DAT	Channel D Serial Data
47	IMCLK	IMCLK	Channel C Serial Clock
48	IMDAT	IMDAT	Channel C Serial Data
50	KCLK	KCLK	Channel B Serial Clock
51	KDAT	KDAT	Channel B Serial Data
52	EMCLK	EMCLK	Channel A Serial Clock
53	EMDAT	EMDAT	Channel A Serial Data

All PS/2 Serial Channel signals (CLK and DAT) are driven by open collector (TYPE I/OD16) drivers pulled to VCC2 (+3.3V nominal) through 10K-ohm resistors.

SMSC PS/2 LOGIC OVERVIEW

The SMSC PS/2 logic allows the host to communicate to any serial auxiliary devices compatible with the PS/2 interface through any one of four channels. The PS/2 Logic consists of four identical SMSC PS/2 channels, each containing a set of four operating registers. The four Channels are PS/2 Chan A, PS/2 Chan B, PS/2 Chan C, and PS/2 Chan D. During a reception, the FDC37N972 latches the data on the high to low transition of the clock. During a transmission, the FDC37N972 transitions the data line on the high to low transition of the clock. See FIGURE 33 - SMSC PS/2 LOGIC BLOCK DIAGRAM.

Notes:

1) Each PS/2 channel has the ability to “busy” the communication link by pulling the clock line low. This is accomplished by simultaneously clearing the PS2_EN and WR_CLK bits in the Control Register.
2) Each PS/2 channel has the ability to abort, prior to the parity bit (10th bit), the transfer in progress.
3) Clock bit time (cycle time) typically varies between 60 and 100 us. The FDC37N972 PS/2 Logic is designed such that it is immune to variations in the clock cycle times within the limit of the transfer timeout.
4) Once a transmission has begun, the PS/2 `peripheral is allowed up to 300us per bit transfer. If the time between falling clock edges exceeds 300us a transfer timeout occurs resulting in either XMIT_TIMEOUT or REC_TIMEOUT being set along with the generation of an interrupt.
5) Once a transmission has started, the PS/2 peripheral has approximately 2ms to complete the transfer. This transfer timeout applies to transmissions as well as receptions. In the case of a transmission(reception), if a 2ms timeout occurs the XMIT_TIMEOUT(REC_TIMEOUT) bit in the status register is set and an interrupt is generated.
6) When the controller is ready to transmit data it floats the data line and drives the clock line low. Once data is written to the Transmit Register the data line is driven low and after a delay the clock line is released (floated) so that the PS/2 peripheral knows data is ready. Releasing the clock signals the start of a trasmission. The PS/2 peripheral has 25ms to acknowledge the transmit start condition above by driving the clock line low. If the PS/2 peripheral does not acknowledge in

the allotted time then a Trasmit timeout occurs: setting the XMIT_TIMEOUT error bit in the Status register and generating an interrupt.

7) By clearing the PS/2 channels PS2_EN bit in its Control Register the PS/2 Channel can be operated in a fully software controlled “Bit-bang” mode. This allows operation of auxilliary devices that do not meet standard PS/2 protocol timing handled by the FDC37N972’s PS/2 Logic block.
8) See Sections 0 through 0 for timing information.

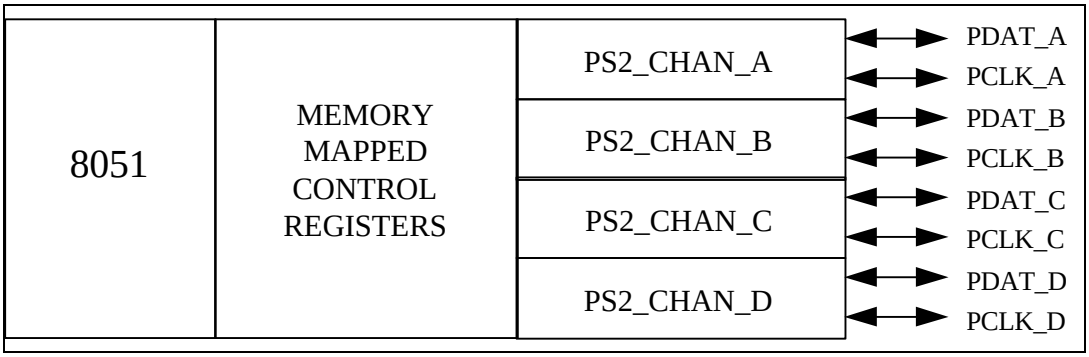


FIGURE 33 - SMSC PS/2 LOGIC BLOCK DIAGRAM

PS/2 DATA FRAME

Data transmissions to and from the auxilliary device connector on each PS/2 channel consist of an 11-bit data stream sent serially over the data line. The following figure shows the function of each bit.

Start Bit Always 0	8 data bits, least sig bit first	Parity Bit Odd on xmit Prog. on rec.	Stop Bit High on xmit Prog. on rec.

FIGURE 34 - PS/2 DEVICE DATA STREAM BIT DEFINITIONS

SMSC PS/2 MEMORY MAPPED CONTROL REGISTERS

Each SMSC PS/2 channel has a separate set of identical control registers: Transmit, Receive, Control,and Status. These are shown in TABLE 86 between addresses 0x7F41 and 0x7F4F. The transmit and receive register share the same address (ie. . PS/2 Chan A Tx/Rx) In addition one register is shared by all four channels to provide RX_Busy indicators.

SMSC PS/2 TRANSMIT REGISTERS

The byte written to this register, when PS2_T/R, PS2_EN, and XMIT_IDLE are set, is transmitted automatically by the PS/2 channel control logic. If any of these three bits (PS2_T/R, PS2_EN, and XMIT_IDLE) are not set, then writes to this

register are ignored. On successful completion of this transmission or upon a Transmit Time-out condition the PS2_T/R bit is automatically cleared and the XMIT_IDLE bit is automatically set. The PS2_T/R bit must be written to a '1' before initiating another transmission to the remote device.

Notes:
1) Even if PS2_T/R, PS2_EN, and XMIT_IDLE are all set, writing the Transmit Register will not kick off a transmission if RDATA_RDY is set. The automatic PS2 logic forces data to be read from the Receive Register before allowing a transmission.
2) An interrupt is generated on the low to high transition of XMIT_IDLE.
3) All bits of this register are write only.

SMSC PS/2 RECEIVE REGISTERS

When PS2_EN=1 and PS2_T/R=0 the PS2 Channel is set to automatically receive data on that channel (both the CLK and DATA lines will float waiting for the peripheral to initiate a reception by sending a start bit followed by the data bits). After a successful reception data is placed in this register and the RDATA_RDY bit is set and the CLK line is forced low by the PS2 channel logic. RDATA_RDY is cleared and the CLK line is released to hi-z following a read of this register. This automatically holds off further receive transfers until the 8051 has had a chance to get the data.

Notes:
1) The Receive Register is initialized to 0xFF after a read or after a Timeout has occured.
2) The channel can be enabled to automatically transmit data (PS2_EN=1) by setting PS2_T/R while RDATA_RDY is set, however a transmission can not be kicked off until the data has been read from the Receive Register.
3) An interrupt is generated on the low to high transition of RDATA_RDY.
4) If a receive timeout (REC_TIMEOUT=1) or a transmit timeout (XMIT_TIMEOUT=1) occurs the channel is busied (CLK held low) for 300us (Hold Time) to guarantee that the peripheral aborts. Writing to the Transmit Register will be allowed, however the data written will not be transmitted until the Hold Time expires.
5) All bits in this register are read only

SMSC PS/2 CONTROL REGISTERS

TABLE 136 - SMSC PS/2 CONTROL REGISTERS (A - D)

HOST ADDRESS	-
8051 ADDRESS	0x7F42 (CHAN A), 0x7F46 (CHAN B), 0x7F4A (CHAN C), 0x7F4E (CHAN D)
POWER	VCC2
DEFAULT	0x40

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	WR_CLK	WR_DATA	STOP		PARITY		PS2_EN	PS2_T/R

Default = 0x40 on VCC2 POR only.

Note: There are four PS/2 Control Registers, one for each channel.

PS2_T/R

PS/2 Channel Transmit/Receive (default = 0). This bit is only valid when PS2_EN=1 and sets the PS2 logic for automatic transmission or reception when PS2_T/R equals '1' or '0' respectively.

When set the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation this bit must be set prior to writing to the Transmit Register; writes are blocked to the Transmit Register when this bit is not set. Upon setting the PS2_T/R bit the channel will drive its CLK line low and then float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS2_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. FDC37N972 drives the data line low and, within 80ns, floats the clock line (externally pulled high by the pull-up resistor) to signal to the external PS/2 device that data is now available. The PS2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Timeout error condition occurs. NOTE: if the PS2_T/R bit is set while the channel is actively receiving data prior to the leading edge of the 10th (parity bit) clock edge the receive data is discarded. If this bit is not set prior to the 10th clock signal then the receive data is saved in the Receive Register.

When the PS2_T/R bit is cleared the PS/2 channel is enabled to receive data. Upon clearing this bit, if RDATA_RDY=0, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission. If the PS2_T/R bit is set while RDATA_RDY=1 then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

PS2_EN

PS2 Channel ENable (default = 0). When PS2_EN=1 the PS/2 State machine is enabled allowing the channel to perform automatic reception or transmission depending on the bit value of PS2_T/R. When PS2_EN = 0, the channel's automatic PS/2 state machine is disabled and the channel can be bit-banged through the WR_DATA and WR_CLK bits in the Contol Register and the RD_DATA and RD_CLK bits in the Status Register. Thus, when PS2_En=0, the channel's CLK and DATA lines are forced to the level specified in the Control Register WR_CLK and WR_DATA bits.

NOTE: If the PS2_EN bit is cleared prior to the leading edge (falling edge) of the 10th (parity bit) clock edge the receive data is discarded (RDATA_RDY remains low). If the PS2_EN bit is cleared following the leading edge of the 10th clock signal then the receive data is saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

PARITY
Bits [3:2] of the Control Register are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits[3:2] = 00 : Receiver expects Odd Parity (default).
= 01 : Receiver expects Even Parity.
= 10 : Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).
= 11 : Reserved.

STOP
Bits [5:4] of the Control Register are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS2_EN=1.

Bits[5:4] = 00 : Receiver expects an active high stop bit.
= 01 : Receiver expects an active low stop bit.
= 10 : Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).
= 11 : Reserved.

WR_DATA
Write DATA bit: When PS2_EN=1, writes to the WR_DATA bit are accepted but result in no action other than setting or clearing this bit. When PS2_EN=0, setting this bit to a 1 or 0 either floats or drives low the PS/2 channel's Serial DATA pin. This bit is used for transmitting bit-banged data over the PS2 channel. Bit-banging of the PS/2 channel is enabled when PS2_EN= 0.

Note : while the Hold timeout is in effect (300us following a Receive or Transmit Timeout) writes to this bit are blocked.

WR_CLK
Write CLK bit: When PS2_EN=1, writes to the WR_CLK bit are accepted but result in no action other than setting or clearing this bit. When PS2_EN=0, setting this bit to a 1 or 0 either floats or drives low the PS/2 channel's Serial CLK pin. Bit-banging of the PS/2 channel is enabled when the PS2_EN bit is set to 0.

Note : While the Hold timeout is in effect (300us following a Receive or Transmit Timeout) writes to this bit are blocked.

Note : When PS2_EN = 0, high to low transitions on the CLK pin caused by the peripheral will generate a PS2 Chan interrupt. A timeout event or writing this bit low will not cause an interrupt.

The default for the WR_DATA bit D6 in the four SMSC PS/2 Control Registers is “1”. The default in earlier devices is “0” (**TABLE 136**). The VCC2 Power-on Default for each Control Register is 40h.

TABLE 137 - SMSC PS/2 STAUS REGISTERS (A - D)

HOST ADDRESS	-
8051 ADDRESS	0x7F43 (CHAN A), 0x7F47 (CHAN B), 0x7F4B (CHAN C), 0x7F4F (CHAN D)
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
BIT NAME	RD_CLK	RD_DATA	XMIT_ TIMEOUT	XMIT_IDLE	FE	PE	REC_ TIMEOUT	RDAT _RDY

Default = 0x40 on VCC2 POR only.

Note: There are four PS/2 Status Registers, one for each channel.

Note : XMIT_TIMEOUT, FE, PE, REC_TIMEOUT, RDATA_RDY are cleared to zero upon a read of this register.

RDATA_RDY

Receive Data Ready: Under normal operating conditions, this bit is set following the falling edge of the 11th clock given successful reception of a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive timeout errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS2_EN bit is cleared following the 10th CLK edge (see the PS2_EN bit description for further details). Reading the Receive Register clears this bit.

Note : An Interrupt is generated on the low to high transition of the RDATA_RDY bit.

REC_TIMEOUT

Under PS2 automatic operation, PS2_EN=1, this bit is set on one of 4 receive error conditions, and in additon the channel's CLK line is automatically pulled low and held for a period of 300us following assertion of the REC_TIMEOUT bit :

1) When the receiver bit time (time between falling edges) exceeds 300us.
2) If the time from the 1st (start) bit to the 10th (parity) bit exceeds 2ms.
3) On a receive parity error along with the parity error (PE) bit.
4) On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit.

The REC_TIMEOUT bit is cleared when the Status Register is read.

Note : An Interrupt is generated on the low to high transition of the REC_TIMEOUT bit.

PE

Parity Error: When receiving data the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel has been set to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an Interrupt is generated.

FE

Framing Error: When receiving data the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel has been set to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an Interrupt is generated.

XMIT_IDLE

Transmiter Idle: When low, the XMIT_IDLE bit is a status bit indicating that the PS2 channel is actively transmitting data to the PS2 peripheral device. Writing to the Transmit Register when the channel is ready to transmit will cause the XMIT_IDLE bit to deassert and remain deasserted until one of the following conditions occur:

1) the falling edge of the 11th CLK; upon a Transmit Timeout condition (XMIT_TIMEOUT goes high);
2) upon the PS2_T/R bit being written to 0;
3) upon the PS2_EN bit being written to 0.

Note : An interrupt is generated on the low to high transition of XMIT_IDLE.

XMIT_TIMEOUT

This bit is set on one of 3 transmit conditions, and in additon the channel's CLK line is automatically pulled low and held for a period of

300us following assertion of the XMIT_TIMEOUT bit during which time the PS2_T/R is also held low :

When the transmitter bit time (time between falling edges) exceeds 300us.
When the transmitter start bit is not received withing 25ms from signaling a transmit start event.
If the time from the 1st (start) bit to the 10th (parity) bit exceeds 2ms.

RD_DATA

Read DATA bit: Reading this bit returns the current level of the PS2 channel's Serial DATA pin. This bit is used for receiving bit-banged data over the PS2 channel. Bit-banging of the PS2 channel is enabled when the PS2_EN bit is set to 0. To receive data properly using this bit, PS2_EN must be set to 0 and the WR_DATA bit in the PS2 Channel's Control Register must be set to 1.

RD_CLK

Read CLK bit: Reading this bit returns the current level of the PS2 channel's Serial CLK pin. This bit is used when receiving bit-banged data over the PS2 channel. Bit-banging of the PS2 channel is enabled when the PS2_EN bit is set to 0. To receive bit banged data properly the PS2_EN must be set to 0 and the WR_CLK bit in the PS2 Channel's Control Register must be set to 1.

Note : When PS2_EN = 0, high to low transitions on the CLK pin will generate a PS2 Chan interrupt. A timeout event or writing this bit low will not cause an interrupt.

Note : When PS2_EN=1, bit-banging is disabled for any of the following 3 conditions:
Time-out is active.
300us following a time-out (Hold Time).
RDATA_RDY = 1.

SMSC PS/2 STATUS_2 REGISTERS

The PS/2_STATUS_2 Register supports the RX_Busy indicators for each of the four PS/2 Channels (A - D) When a RX_BUSY bit is set the associated channel is actively receiving PS/2 data; when a RX_BUSY bit is clear the channel is idle.

TABLE 138 - SMSC PS/2_STATUS_2 REGISTER

HOST ADDRESS`	-
8051 ADDRESS	0x7F48
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R

PROGRAMMER'S NOTE:

Always check that an SMSC PS/2 channel is idle, i.e. the RX_BUSY bit is "0", before attempting to transmit on that channel. Receive data may or may not be lost by setting an SMSC PS/2 channel to transmit while the RX_BUSY bit is asserted depending where in the message frame the tranmit mode change occurs.

DEVIL LOGIC OVERVIEW

The Devil PS/2 logic allows the host to communicate to any serial auxiliary devices compatible with the PS/2 interface through any one of four ports: EM, KB, IM and PS2. There are two identical PS/2 channels, each containing a set of five operating registers. Channel 1 (PS/2 Port 1) consists of ports EM and KB and channel 2 (PS/2 Port 2) consists of ports IM and PS2. The FDC37N972 latches data on the high to low transition of the clock.

THE DEVIL PS/2 LOGIC COMMANDS

The Devil PS/2 logic supports three commands: Transmit, Receive, and Inhibit.

Notes:

1) The hardware state machine requires that you read any pending command response byte from the input register before you send an Inhibit command to the device. Since only one response byte is allowed to be automatically received, there is no need to inhibit the port before you read the response.
2) After sending a Transmit or Receive command to the Control register, do not read the status register until the PS/2 Interrupt Flag is set. If you read the status register to check the BUSY bits, the bit counter will reset and you will either get receive time-outs (all bits not received within 2 ms), or you will get parity errors. If there is a receive error, the BUSY bit can be used to determine which device was sending when the error occurred. If there is a transmit error, the ENABLE bit in the Control register can be used to determine which device was selected.
3) If your PS/2 code is interrupt driven, is best to send the inhibit command while the interrupts are enabled so any byte being received can finish and get picked up by the interrupt handler. This is necessary because a receive may have been in progress when the Inhibit command was issued, and a receive will complete if the parity bit is reached.
4) If there is a Request To Send (RTS) time-out or other condition which results in no byte being received from the DEVIL PS/2 device, there will be no device 'data ready' flag set in the status register. It will be necessary to read the device enable bits in the status register, or use some other means to remember which.

THE DEVIL PS/2 LOGIC TRANSMIT COMMAND

The Devil PS/2 serial protocol requires that the auxiliary device respond to all transmissions that it receives. The response is usually a 0xFA , 0xFE, 0xFC or 0xEE. The response is stored in the DEVIL PS/2 ports RECEIVE register. Thus, after each transmission the RECEIVE register should contain some response byte.

When sending a byte to a DEVIL PS/2 device, Two writes to the control register are required to avoid race conditions: first the device select bit(s) (bits[4:3]) in the control register must be set, clearing the command bits[2:0]; then another write to the control register selecting

ONE command, and preserving the device select bits. The DEVIL PS/2 logic will assume that the byte being sent is a 'command', and will automatically go into receive mode for a single response byte. The DEVIL PS/2 logic must be placed into receive mode to receive additional response bytes. An error will be reported if the device does not start clocking out the command byte within 15 ms, or if the device does not send a response within 32 ms of receiving the command. The DEVIL PS/2 logic will cause an interrupt after the response byte is received, or if there is a send or receive time-out.

The DEVIL PS/2 logic drives the clock line low and then floats the data line when the port is selected to transmit. Writing to the TRANSMIT register initiates the transmit operation. The data line is driven low and, within 80ns, the clock line is floated (externally pulled high by the pull-up resistor). The auxiliary device recognizes this as the start bit, and responds by providing the eleven clocks (each clock corresponds to a bit). The Logic provides a 3.2µS bit hold time. If the auxiliary device did not respond within 15 mS after the start bit, transmit is terminated and ERROR bit of the STATUS register and the RTSTIMOUT bit of the ERROR register are set. The auxiliary device has 2 ms to complete the transmission or the DEVIL PS/2 logic will set the ERROR bit of the STATUS register and the XMTTIMOUT bit of the ERROR register. If the transmission is successful, the clock and data lines are floated waiting for the auxiliary device to send the response packet. If the first byte of the response packet is not received within 32 mS, the ERROR bit of the STATUS register is set, the RESTIMOUT bit of the ERROR register is set. If, on the other hand, the response packet is received and there are no errors, the DEVIL PS/2 logic sets the READY bit of the STATUS register, clears the ERROR bit of the STATUS register, and clears the ERROR register. The RECEIVE register contains the received response byte.

THE DEVIL PS/2 LOGIC RECEIVE COMMAND

When receiving scan codes or mouse packets, select one or both DEVIL PS/2 devices in the Control register (bits[4:3]), clearing the command bits[2:0]. Then do another write setting the Receive command bit while preserving the device select bits. The DEVIL PS/2 logic will only let one device send at a time (whichever starts sending first), and will cause an interrupt for each received byte. Reading the byte from the Receive register causes the DEVIL PS/2 logic to go into receive mode again.

The DEVIL PS/2 logic floats the DEVIL PS/2 port's clock and data line when the port is selected to receive. The auxiliary device initiates the transfer by driving the data line low and 12µS later driving the clock low. The DEVIL PS/2 Logic recognizes this as a start bit and sets the BUSY bit. The auxiliary device proceeds by transmitting ten more bits to the DEVIL PS/2 logic. The DEVIL PS/2 Logic latches the data on the high to low transition of the clock. After the stop bit, the DEVIL PS/2 Logic clears the BUSY bit and drives the clock line low until the RECEIVE register is read by the 8051. If there is no error in the transfer, the DEVIL PS/2 logic sets the READY bit of the STATUS register, clears the ERROR bit of STATUS register, and clears the ERROR register. If, however, the receive operation does not complete in 2 ms of receiving a start bit, the ERROR bit of the STATUS register is set together with the RECTIMOUT bit of the ERROR register, and the READY bit is not set.

Note that the logic can be left in receive mode indefinitely and is normally used to receive keyboard scan codes and mouse packets.

THE DEVIL PS/2 LOGIC INHIBIT COMMAND

When you abort a transmission from a DEVIL PS/2 device, it is necessary to hold the clock line low for at least 100 us in order for the device to note that the transmission has been aborted. This 100 us low clock time is called a device 'Inhibit'. When you want to perform the Inhibit command, select one or both DEVIL PS/2 devices in the Control register, clearing the command bits. Then do another write setting the Inhibit command bit while preserving the device select bits. The DEVIL PS/2 logic will hold the device clock lines low and count down 100 us, then it will generate an interrupt to indicate that the time-out is over. The interrupt handler should then clear the Inhibit command bit in the Control register. After an Inhibit, the device clock lines will remain low until the next Transmit or Receive command.

Note that if the device is receiving a byte when the Inhibit command is sent, and the parity bit has already been started, the device will complete the receipt and set the READY bit before the inhibit takes effect, so it is necessary to check for data even when the INHIBIT DONE bit is set.

DEVIL PS/2 MEMORY MAPPED CONTROL REGISTERS

Each Devil PS/2 channel has a separate set of identical control registers: Control, Status, Error Status, Transmit, and Receive. These are shown in TABLE 86 between addresses 0x7F41 and 0x7F4F.

DEVIL PS/2 CONTROL REGISTERS

TABLE 139 - DEVIL PS/2 CONTROL REGISTERS (PORT1 & PORT2)

HOST ADDRESS	-
8051 ADDRESS	0x7F41 (PORT 1), 0x7F49 (PORT 2),
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME Port1 (Port2)	Res	Res	Res	EM_EN (IM_EN)	KB_EN (PS2_EN)	Inhibit	RX_EN	TX_EN

TABLE 140 - PS/2 PORT1 (PORT2) CONTROL REGISTER OPERATION

Inhibit	RX_EN	TX_EN	EM_EN (IM_EN)	KB_EN (PS2_EN)	OPERATION STATUS
0	0	1	0	1	Transmission sent to Keyboard, echo cmd received
0	0	1	1	0	Transmission sent to Ext Mouse, echo cmd rcvd
0	0	1	1	1	Transmission inhibited, RTS_timeout error, (illegal state)
0	1	0	0	1	Data received from Keyboard, Transmission initiated by Keyboard.
0	1	0	1	0	Data received from Mouse, Transmission initiated by Mouse.
0	1	0	1	1	Data received from Keyboard and Mouse, transmissions are initiated by Keyboard and Mouse and interlaced to PS/2 Port1 receive register.
1	X	X	X	X	EM and KB PS/2 interfaces are disabled. Data written to the PS2 Port1 transmit register is not transmitted and no data is received from the external Mouse or Keyboard.

Notes:

1. The operation of the PS/2 Port2 control register is similar for the IM and PS/2 devices.
2. Only one of bits D2-D0 can be set to one.

DEVIL PS/2 STATUS REGISTERS

TABLE 141 - DEVIL PS/2 STATUS REGISTERS (PORT1 & PORT2)

HOST ADDRESS	-
8051 ADDRESS	0x7F42 (PORT 1), 0x7F4A (PORT 2),
POWER	VCC2
DEFAULT	0x40

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT NAME Port1 (Port2)	Res	Res	EM_busy (IM_busy)	KB_busy (PS2_busy)	Inhibit done	EM_drdy (IM_drdy)	KB_drdy (PS2_drdy)	Error

ERROR

This bit is set in the event of a transmit or receive error condition on either the EM or KB PS/2 ports or the IM or PS/2 ports. The cause of the error can be determined by reading the PS/2 Port1 or PS/2 Port2 Status register.

KB_DRDY

This bit is set if KB_EN is set and a character has been received successfully from the PS/2 KB port. This bit is cleared when the data has been read from the PS/2 Port1 Receive register.

EM_DRDY

This bit is set if EM_EN is set and a character has been received successfully from the PS/2 EM port. This bit is cleared when the data has been read from the PS/2 Port1 Receive register.

PS2_DRDY

This bit is set if PS2_EN is set and a character has been received successfully from the PS/2 port. This bit is cleared when the data has been read from the PS/2 Port2 Receive register.

IM_DRDY

This bit is set if IM_EN is set and a character has been received successfully from the PS/2 IM port. This bit is cleared when the data has been read from the PS/2 Port2 Receive register.

INHIBIT DONE
This bit is set when the INHIBIT bit of the CONTROL register was set and the 100 uS inhibit sequence has finished.

KB_BUSY

This bit is set when the PS/2 KB port is actively receiving a character.

EM_BUSY

This bit is set when the PS/2 EM port is actively receiving a character.

PS2_BUSY

This bit is set when the PS/2 port is actively receiving a character.

IM_BUSY

This bit is set when the PS/2 IM port is actively receiving a character.

Note:
1) On receive the BUSY bit is set while receiving the first data bit and cleared while receiving the parity bit. On transmit, the BUSY bit is not set at all.
2) The operation of the PS/2 Port2 status register is similar for the IM and PS/2 devices.

DEVIL PS/2 ERROR STATUS

TABLE 142 - DEVIL PS/2 ERROR STATUS REGISTERS (PORT1 & PORT2)

HOST ADDRESS	-
8051 ADDRESS	0x7F43(PORT 1), 0x7F4B(PORT 2),
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R
BIT NAME	Res	Res	Res	Parity	RES_ timeout	REC_ timeout	RTS_ timeout	XMT_ timeout

XMT_TIMEOUT

(Transmit_timeout) is set when the device fails to clock out a command within 2ms of clocking out the start bit.

RTS_TIMEOUT

(ReadyToSend_timeout) is set when the device fails to start clocking out the command within 15 ms.

REC_TIMEOUT

(RECeiver_timeout) is set when the device does not finish sending a byte within 2 ms of sending the start bit.

RES_TIMEOUT

(RESponse_timeout) is set when the response to a command is not received within 32 ms.

PARITY

The PS/2 ports use Odd parity, in the event of a receive parity error this bit is set.

DEVIL PS/2 TRANSMIT REGISTERS

TABLE 143 - DEVIL PS/2 TRANSMIT REGISTERS (PORT1 & PORT2)

HOST ADDRESS	-
8051 ADDRESS	0x7F44(PORT 1), 0x7F4C(PORT 2),
POWER	VCC2
DEFAULT	0x00

The byte written to the PS/2 Port1(Port2) Transmit register is immediately transmitted onto the enabled PS/2 Port1/Port2 provided that the PS/2 Port1(Port2) Inhibit bit is not set and that both PS/2 Port1and Port2 devices are not enabled for transmit at the same time. This register is write only.

DEVIL PS/2 RECEIVE REGISTERS

TABLE 144 - DEVIL PS/2 RECEIVE REGISTERS (PORT1 & PORT2)

HOST ADDRESS	-
8051 ADDRESS	0x7F45(PORT 1), 0x7F4D(PORT 2),
POWER	VCC2
DEFAULT	0x00

If KB_EN, and/or EM_EN is set and PS/2 Port1 RX_EN is set any successfully received characters over the KB and/or the EM PS/2 Port are placed into this register and the EM_drdy or KB_drdy PS/2 Port1 status bit is set. Similarly, if PS2_EN and/or IM_EN is set and PS/2 Port2 RX_EN is set any successfully received characters over the PS2 and/or IM PS2 Ports are placed into this register and the PS2_drdy or IM_drdy PS/2 Port2 status bit is set.

ACCESS.BUS

The FDC37N972 supports ACCESS.bus. ACCESS.bus is a serial communication protocol between a computer host and its peripheral devices. It provides a simple, uniform and inexpensive way to connect peripheral devices to a single computer port. A single ACCESS.bus on a host can accommodate up to 125 peripheral devices.

The ACCESS.bus protocol includes a physical layer based on the I^2C^{TM} serial bus developed by Philips, and several software layers. The software layers include the base protocol, the device driver interface, and several specific device protocols.

BACKGROUND

For a description of the ACCESS.bus protocol, please refer to the ACCESS.bus Specifications Version 2.2, February 1994, available from the ACCESS.bus Industry Group (ABIG).

The ACCESS.bus interface is based on the PCF8584 controller. The registers are mapped into the 8051's external memory mapped register space. The addresses for the registers are shown in **TABLE 145 - ACCESS.BUS REGISTER ADDRESSES.**

TABLE 146 - ACCESS.BUS REGISTER ADDRESSES

ADDRESS (NOTE 1)	ACCESS RIGHTS	REGISTER	
7F31h	W	Control	S1
7F31h	R	Status	S1
7F32h	R/W	Own Address	S0'
7F33h	R/W	Data	S0
7F34h	R/W (1)	Clock	S2

Note: These Registers are only directly accessible by the 8051 and reside within the 8051's external Memory Mapped Data address space.

Note 1: Bits 2 through 6 are read only reserved.

REGISTER DESCRIPTION

The ACCESS.bus interface has four internal register locations. Two of these, Own Address register S0' and Clock register S2, are used for initialization of the chip. Normally they are only written once directly after resetting of the chip. The other two registers, the Data register S0, and the Control/Status register S1, (which functions as a double register) are used during actual data transmission/reception. Register s0 performs all serial-to-parallel interfacing with the ACCESS.bus. Register S1 contains ACCESS.bus status information required for bus access and/or monitoring.

ACCESS.BUS CONTROL/STATUS REGISTER S1

The control/status register controls the ACCESS.bus operation and provides status information. This register has separate read and write functions for all bit positions. The write-only section provides register access control and control over ACCESS.bus signals, while the read-only section provides ACCESS.bus status information.

ACCESS.BUS CONTROL/STATUS REGISTER S1:

CONTROL	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	W	W	W	W	W	W	W	W
Bit Def	PIN	ES0	Reserved	Reserved	ENI	STA	STO	ACK
Status	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
R/W	R	R	R	R	R	R	R	R
Bit Def	PIN	0	STS	BER	LRB	AAS	LAB	nBB

BIT DEFINITIONS
REGISTER S1 CONTROL SECTION

The write-only sections of S1 enables access to registers S0, S1 and S2, and also control of ACCESS.bus operation.

BIT 7 PIN

Pending Interrupt Not. Writing the PIN bit to a logic "1" deasserts all status bits except for the nBB (Bus Busy) - nBB is not affected. The PIN bit is a self-clearing bit. Writing this bit to a logic "0" has no effect. This may serve as a software reset function.

BIT 6 ESO

Enable Serial Output. ESO enables or disables the serial ACCESS.bus I/O. When ESO is high, ACCESS.bus communication is enabled; communication with serial shift register S0 is enabled and the S1 bus status bits are made available for reading. With ESO = 0, bits ENI, STA, STO and ACK of S1 can be read for test purposes.

BIT 5 and 4 Reserved

BIT 3 ENI

This bit enables the internal interrupt, nINT, which is generated when the PIN bit is active (logic 0).

BIT 2 and 1 STA and STO

These bits control the generation of the ACCESS.bus Start condition and transmission of slave address and R/nW bit, generation of repeated Start condition, and generation of the STOP condition (see TABLE 147).

TABLE 147 - INSTRUCTION TABLE FOR SERIAL BUS CONTROL

STA	STO	PRESENT MODE	FUNCTION	OPERATION
1	0	SLV/REC	START	Transmit START+address, remain MST/TRM if R/nW=0; go to MST/REC if R/nW=1.
1	0	MST/TRM	REPEAT START	Same as for SLV/REC
0	1	MST/REC; MST/TRM	STOP READ; STOP WRITE	Transmit STOP go to SLV/REC mode; Note 1
1	1	MST	DATA CHAINING	Send STOP, START and address after last master frame without STOP sent; Note 2
0	0	ANY	NOP	No operation; Note 3

Note 1: In master receiver mode, the last byte must be terminated with ACK bit high ('negative acknowledge').

Note 2: If both STA and STO are set high simultaneously in master mode, a STOP condition followed by a START condition + address will be generated. This allows 'chaining' of transmissions without relinquishing bus control.

Note 3: All other STA and STO mode combinations not mentioned in **TABLE 146** are NOPs.

BIT 0 ACK

This bit must be set normally to logic "1". This causes the ACCESS.bus to send an acknowledge automatically after each byte (this occurs during the 9th clock pulse). The bit must be reset (to logic "0") when the ACCESS.bus controller is operating in master/receiver mode and requires no further data to be sent from the slave transmitter. This causes a negative acknowledge on the ACCESS.bus, which halts further transmission from the slave device.

REGISTER S1 STATUS SECTION

The read-only section of S1 enables access to ACCESS.bus status information.

BIT 7 PIN

Pending Interrupt Not. This bit is a status flag which is used to synchronize serial communication and is set to logic "0" whenever the chip requires servicing. The PIN bit is normally read in polled applications to determine when an ACCESS.bus byte transmission/reception is completed.

When acting as transmitter, PIN is set to logic "1" (inactive) each time S0 is written. In receiver mode, the PIN bit is automatically set to logic "1" each time the data register S0 is read.

After transmission or reception of one byte on the ACCESS.bus (nine clock pulses, including acknowledge) the PIN bit will be automatically reset to logic "0" (active) indicating a complete byte transmission/reception. When the PIN bit is subsequently set to logic "1" (inactive) all status bits will be reset to "0" on a BER (bus error) condition.

In polled applications, the PIN bit is tested to determine when a serial transmission/reception has been completed. When the ENI bit (bit 4 of write-only section of register S1) is also set to logic "1" the hardware interrupt is enabled. In this case, the PI flag also triggers and internal

interrupt (active low) via the nINT output each time PIN is reset to logic “0”.

When acting as a slave transmitter or slave receiver, while PIN = “0”, the chip will suspend ACCESS.bus transmission by holding the SCL line low until the PIN bit is set to logic “1” (inactive). This prevents further data from being transmitted or received until the current data byte in S0 has been read (when acting as slave receiver) or the next data byte is written to S0 (when acting as slave transmitter).

PIN BIT SUMMARY

The PIN bit can be used in polled applications to test when a serial transmission has been completed. When the ENI bit is also set, the PIN flag sets the internal interrupt via the nINT output.

In transmitter mode, after successful transmission of one byte on the ACCESS.bus the PIN bit will be automatically reset to logic “0” (active) indicating a complete byte transmission.

In transmitter mode, PIN is set to logic “1” (inactive) each time register S0 is written. In receiver mode, PIN is set to logic “0” (inactive) on completion of each received byte. Subsequently, the SCL line will be held low until PIN is set to logic “1”.

In receiver mode, when register S0 is read, PIN is set to logic “1” (inactive).

In slave receiver mode, an ACCESS.bus STOP condition will set PIN=0 (active).

PIN=0 if a bus error (BER) occurs.

BIT 6 RESERVED, Logic 0.

BIT 5 STS

When in slave receiver mode, this flag is asserted when an externally generated STOP condition is detected (used only in slave receiver mode).

BIT 4 BER

Bus error; a misplaced START or STOP condition has been detected. Resets nBB (to logic “1”; inactive), sets PIN = “0” (active).

BIT 3 LRB/AD0

Last Received Bit or Address 0 (general call) bit. This status bit serves a dual function, and is valid only while PIN=0: LRB holds the value of the last received bit over the ACCESS.bus while AAS=0 (not addressed as slave). Normally this will be the value of the slave acknowledgment; thus checking for slave acknowledgment is done via testing of the LRB.
ADO; when AAS = “1” (Addressed as slave condition) the ACCESS.bus controller has been addressed as a slave. Under this condition, this bit becomes the AD0 bit and will be set to logic “1” if the slave address received was the ‘general call’ (00h) address, or logic “0” if it was the ACCESS.bus controller’s own slave address.

BIT 2 AAS

Addressed As Slave bit. Valid only when PIN=0. When acting as slave receiver, this flag is set when an incoming address over the ACCESS.bus matches the value in own address register S0’ (shifted by one bit) or if the ACCESS.bus ‘general call’ address (00h) has been received (‘general call’ is indicated when AD0 status bit is also set to logic “1”).

BIT 1 LAB

Lost Arbitration Bit. This bit is set when, in multi-master operation, arbitration is lost to another master on the ACCESS.bus.

BIT 0 NBB

Bus Busy bit. This is a read-only flag indicating when the ACCESS.bus is in use. A zero indicates that the bus is busy, and access is not possible. This bit is set/reset (logic "1"/logic "0") by Start/Stop conditions.

OWN ADDRESS REGISTER S0'

When the chip is addressed as slave, this register must be loaded with the 7-bit ACCESS.bus address to which the chip is to respond. During initialization, the own address register S0' must be written to, regardless whether it is later used. The Addressed As Slave (AAS) bit in status register S1 is set when this address is received (the value in S0 is compared with the value in S0'). Note that the S0 and S0' registers are offset by one bit; hence, programming the own address register S0' with a value of 55h will result in the value AAh being recognized as the chip's ACCESS.bus slave address.

After reset, S0' has default address 00h.

TABLE 148 - ACCESS.BUS OWN ADDRESS REGISTER S0

OWN ADDR	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Def	Reserved	Slave Address 6	Slave Address 5	Slave Address 4	Slave Address 3	Slave Address 2	Slave Address 1	Slave Address 0

DATA SHIFT REGISTER S0

Register S0 acts as serial shift register and read buffer interfacing to the ACCESS.bus. All read and write operations to/from the ACCESS.bus are done via this register. ACCESS.bus data is always shifted in or out of shift register S0.

In receiver mode the ACCESS.bus data is shifted into the shift register until the acknowledge phase. Further reception of data is inhibited (SCL held low) until the S0 data shift register is read.

In the transmitter mode data is transmitted to the ACCESS.bus as soon as it is written to the S0 shift register if the serial I/O is enabled (ESO=1).

TABLE 149 - ACCESS.BUS DATA REGISTER S0

DATA	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CLOCK REGISTER S2

Register S2 controls the selection of the internal chip clock frequency used for the ACCESS.bus block. This determines the SCL clock frequency generated by the chip. The selection is made via Bits[2:0] (see Table 151 - INTERNAL CLOCK RATES AND ACCESS.BUS DATA RATES).

TABLE 150 - ACCESS.BUS CLOCK REGISTER

	D7	D6-D2	D1	D0
8051 R/W	R/W	R	R/W	R/W
	AB_RST (Note 1)	Reserved	00 - clock off (default) 01 - 32 kHz clock 10 - 8051 clock 11 - 24 MHz clock (see table below)	

Note 1: ACCESS.bus Reset, not self-clearing, must be written high and then written low. Bit 7 AB_RST: (ACCESS.bus Reset) setting this bit re-initializes all logic and registers in the ACCESS.bus block.

TABLE 151 - INTERNAL CLOCK RATES AND ACCESS.BUS DATA RATES

ACCESS BUS CLOCK	CLOCK RATE	DATA RATE	NOMINAL HIGH	NOMINAL LOW	MINIMUM HIGH
D[1-0]					
00	Off				
10	Ring Osc	f/240	96/f	144/f	18/f
	Ring Osc=4 MHz	16.7 kHz	24µs	36µs	4.5µs
	Ring Osc=6 MHz	25 kHz	16µs	24µs	3µs
	Ring Osc=8 MHz	33.3 kHz	12µs	18µs	2.25µs
10	12MHz	50 kHz	8µs	12µs	4µs
10	14.3 MHz	60 kHz	6.7µs	10.1µs	4µs
10	16 MHz	67 kHz	6µs	9µs	4µs
11	24 MHz	100 kHz	4µs	6µs	4µs

f = frequency of the ring oscillator.

ACCESS.BUS INTERFACE DESCRIPTION

The ACCESS.Bus interface is fully and directly controlled by the on-chip 8051 through its set of on-chip memory mapped control registers. The ACCESS.bus logic is based on the PCF8584 I2C controller and is powered on the VCC1 powerplane to provide the ability to wake-up the 8051 on an ACCESS.bus event.

MEMORY MAPPED CONTROL REGISTERS

TABLE 152 - ACCESS.BUS CONTROL REGISTER

Host	N/A
8051	0x7F31 (W)
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	W	W	W	W	W	W	W	W
Bit Def	PIN	ES0	Reserved	Reserved	ENI	STA	STO	ACK

Bit 7 PIN: Pending Interrupt Not - Writing this bit to a logic “1” deasserts all status bits except for nBB (Bus
Busy), nBB is not affected. This is a self-clearing bit. Writing this bit to a logic “0” has no effect.

TABLE 153 - ACCESS.BUS STATUS REGISTER

Host	N/A
8051	0x7F31 (R)
Power	VCC1
Default	0x81

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	R	R	R	R	R	R	R	R
Bit Def	PIN	0	STS	BER	LRB	AAS	LAB	NBB

ACCESS.BUS OWN ADDRESS REGISTER

Host	N/A
8051	0x7F32
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Def	Reserved	Slave Address 6	Slave Address 5	Slave Address 4	Slave Address 3	Slave Address 2	Slave Address 1	Slave Address 0

ACCESS.BUS DATA REGISTER

Host	N/A
8051	0x7F33
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ACCESS.BUS CLOCK REGISTER

Host	N/A
8051	0x7F34
Power	VCC1
Default	0x00

ACCESS.BUS CLOCK

	D7	D6-D2	D1	D0
8051 R/W	R/W	R	R/W	R/W
	AB_RST*	Reserved	00 - clock off (default) 10 - 8051 clock 11 - 24 MHz clock	

(*) ACCESS.bus Reset, not self-clearing, must be written high and then written low.

Bit 7 AB_RST: (ACCESS.bus Reset) setting this bit re-initializes all logic and registers in the ACCESS.bus block.

TABLE 154 - ACCESS.BUS CLOCK RATES

ACCESS. bus CLOCK	CLOCK RATE	DATA RATE	NOMINAL HIGH	NOMINAL LOW	MINIMUM HIGH
D[1:0]					
00	Off				
10	Ring Osc	f/240	96/f	144/f	18/f
	Ring Osc=4 MHz	16.7 kHz	24µs	36µs	4.5µs
	Ring Osc=6 MHz	25 kHz	16µs	24µs	3µs
	Ring Osc=8 MHz	33.3 kHz	12µs	18µs	2.25µs
10	12 MHz	50 kHz	8µs	12µs	4µs
10	14.3 MHz	60 kHz	6.7µs	10.1µs	4µs
10	16 MHz	67 kHz	6µs	9µs	4µs
11	24 MHz	100 kHz	4µs	6µs	4µs

f = frequency of the ring oscillator.

SECOND I²C BUS INTERFACE

OVERVIEW

A second I²C controller (ACCESS.bus 2) is in the FDC37N972. ACCESS.bus 2 is powered by VCC1. There are 5 Memory-Mapped Control Registers to support the ACCESS.bus 2 controller (TABLE 155 to TABLE 159).

The two ACCESS.bus 2 controller pins, AB2_DATA and AB2_CLK, are multiplexed on GPIO11 and GPIO12 (see **MULTIFUNCTION PIN** on page 271). An I²C input clock divider bit D2 is added to the ACCESS.bus CLOCK registers (see section 0 I2C Clock Divider *BIT*, below).

MEMORY MAPPED CONTROL REGISTERS

TABLE 155 - ACCESS.BUS 2 CONTROL REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F67 (W)	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	**W**	**W**	**W**	**W**	**W**	**W**	**W**	**W**
BIT NAME	PIN	ES0	RESERVED		ENI	STA	STO	ACK

TABLE 156 - ACCESS.BUS 2 STATUS REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F67 (R)	VCC1	0x81

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R**
BIT NAME	PIN	0	STS	BER	LRB	AAS	LAB	nBB

TABLE 157 - ACCESS.BUS 2 OWN ADDRESS REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F68	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RESERVED	SLAVE ADDR. 6	SLAVE ADDR. 5	SLAVE ADDR. 4	SLAVE ADDR. 3	SLAVE ADDR. 2	SLAVE ADDR. 1	SLAVE ADDR. 0

TABLE 158 - ACCESS.BUS 2 DATA REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F69	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0

TABLE 159 - ACCESS.BUS 2 CLOCK REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F6A	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	**R/W**	**R**	**R**	**R**	**R**	**R**	**R/W**	**R/W**
BIT NAME	AB_RST	RESERVED				CLK_DIV	CLOCK SELECT	

I²C CLOCK DIVIDER BIT

An input clock divider bit D2 is added to the ACCESS.bus CLOCK registers 0x7F34 (TABLE 160) and 0x7F6A (TABLE 159). The clock divider bit CLK_DIV affects all I²C clock inputs. When CLK_DIV is "1", the I²C input clock is divided by 2. When CLK_DIV is "0", the I²C input clock is not divided.

TABLE 160 - ACCESS.BUS 1 CLOCK REGISTER

HOST ADDRESS	n/a
8051 ADDRESS	0x7F34
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R	R	R	R	R/W	R/W	R/W
BIT NAME	AB_RST	RESERVED				CLK_DIV	CLOCK SELECT	

CLOCK SELECT ENCODING

The encoding for the two CLOCK SELECT bits is shown in **Table 161.** The CLOCK SELECT bits are located in the ACCESS.bus 1 Clock Register (**TABLE 160**) and the ACCESS.bus 2 Clock Register (**TABLE 159**).

TABLE 161 - ACCESS.BUS CLOCK SELECT BIT ENCODING

CLOCK SELECT BITS		FDC37N972
D1	D0	
0	0	CLOCK OFF
0	1	RESERVED
1	0	8051 CLOCK
1	1	24 MHz CLOCK

MAILBOX REGISTER INTERFACE

OVERVIEW

The Mailbox Registers Interface provides a standard run-time mechanism for the host to communicate with the 8051 and other logical components in the FDC37N972. The Mailbox Registers Interface includes a total of 44 index-addressable 8-bit registers (TABLE 162) and two 8-bit host access ports (TABLE 164). Thirty-two of these 44 registers are 8051 Mailbox registers.

The Mailbox Registers Interface host access ports are run-time registers that occupy two addresses in the system I/O space. The access ports are used by the host to read and write the 44 registers. The access ports base address is determined by the Mailbox Registers Interface Base Address that is initialized in Logical Device Number 9 in FDC37N972 configuration registers CR60 and CR61 (TABLE 163).

The 32 Mailbox registers as well as the PWM0, PWM1, and Fan Control registers are directly addressable by the 8051 through Memory-Mapped Control Registers (see TABLE 86 - 8051 ON-CHIP EXTERNAL MEMORY MAPPED REGISTERS on page 159). In this specification, the registers in the Mailbox Registers Interface are identified by the prefix MBX in front of a hexadecimal index address. TABLE 162 below summarizes the 44 registers in the Mailbox Registers Interface.

TABLE 162 - MAILBOX REGISTERS INTERFACE

	TOTAL REGS.	MAILBOX INDEX ADDRESS	SYSTEM R/W	8051 ADDR. (7F00+)	8051 R/W	POWER PLANE	VCC 1 POR	VCC 2 POR	ZERO WAIT STATE (1)	NOTES
System-to-8051 Mailbox register 0	1	MBX82h	R/W	08h	RC	VCC1	00		Y	2
8051-to-system Mailbox register 1	1	MBX83h	RC	09h	R/W	VCC1	00		Y	3
Mailbox register [2-F]	14	MBX 84h-91h	R/W	0Ah - 17h	R/W	VCC1	00h		Y	
PWM0 register	1	MBX92h	R/W	25h	R/W	VCC1	00h		Y	
PWM1 register	1	MBX93h	R/W	26h	R/W	VCC1	00h		Y	
8051STP_CLK	1	MBX94h	R/W	-	-	VCC1	00h		Y	4
HMEM	1	MBX95h	R/W	-	-	VCC1	07h	07 h	Y	4, 5
ESMI source register	1	MBX96h	R/W	-	-	VCC2		00h	Y	
ESMI mask	1	MBX97h	R/W	-	-	VCC2		00h	Y	

	TOTAL REGS.	MAILBOX INDEX ADDRESS	SYSTEM R/W	8051 ADDR. (7F00+)	8051 R/W	POWER PLANE	VCC 1 POR	VCC 2 POR	ZERO WAIT STATE (1)	NOTES
register										
IR data register	1	MBX98h	R/W	-	-	VCC2		00h	Y	
Force Disk Change register	1	MBX99h	R/W	-	-	VCC2		03h	Y	
Floppy Data Rate Select Shadow register	1	MBX9Ah	R	-	-	VCC2		N/A	Y	
UART1 FIFO Control Shadow register	1	MBX9Bh	R	-	-	VCC2		00h	Y	
UART2 FIFO Control Shadow register	1	MBX9Ch	R	-	-	VCC2		00h	Y	
Fan Control Register	1	MBX9Dh	R/W	28h	R/W	VCC1	0x30		Y	
Mailbox Register [10-1F]	16	MBX A0h-AFh	R/W	70h – 7Fh	R/W	VCC1	00h		Y	
	44									

NOTES:

1. When accessed for a read or write by the System the registers marked with a “Y” will drive the Zero wait state pin active.
2. Interrupt is cleared when read by the 8051
3. Interrupt is cleared when read by the host
4. When IRESET_OUT is cleared (written from “1” to”0”) 8051STP_CLK bit D0 as well as HMEM bits D1 and D0 are all set to “1”.
5. These registers are reset 500us to 1ms following the condition that BOTH VCC2 is valid and PWRGD is asserted given that the RTC is in normal mode and the VRT bit is set (refer to the RTC section). If the RTC is not in normal mode and/or the VRT bit is not set then these registers are reset within 10us following the condition that BOTH VCC2 is valid and PWRGD is asserted.

MAILBOX REGISTERS INTERFACE BASE ADDRESS

Logical Device 9 in the FDC37N972 configuration space supports the Mailbox Registers Interface. The three device configuration registers in LDN9 provide activation control and the base address for the Mailbox Registers Interface run-time registers (TABLE 163).

Register 0x30 is the Activate register. The activation control (LDN9:CR30.0) qualifies address decoding for the Mailbox Registers Interface; e.g., if the Activate bit D0 in the Activate register is "0", the MBX access port addresses will not be decoded; if the Activate bit is "1", MBX access port addresses will be decoded depending on the values programmed in the MBX Primary Base Address registers.

Registers 0x60 and 0x61 are the MBX Primary Base Address registers. Register 0x60 is the MBX Primary Base Address High Byte, register 0x61 is the MBX Primary Base Address Low Byte.

NOTE: Bit D0 in the MBX Primary Base Address Low Byte must be "0". Valid Mailbox Registers Interface Base Address values are 0x0000 – 0x0FFE.

TABLE 163 - MAILBOX REGISTERS INTERFACE CONFIGURATION CONTROLS (LDN9)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1 & VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							
						RESERVED							Activate
0x60	R/W	0x00	0x00	0x00	-	MBX Primary Base Address High Byte							
						"0"	"0"	"0"	"0"	A11	A10	A9	A8
0x61	R/W	0x00	0x00	0x00	-	MBX Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	A2	A1	"0"

MAILBOX REGISTERS INTERFACE ACCESS PORTS

The Mailbox registers access ports are runtime registers that occupy two addresses in the Host I/O space (TABLE 164).

To access a Mailbox register once the Mailbox Registers Interface Base Address has been initialized, write the Mailbox register index address to the MBX Index port and read or write the Mailbox register data from the MBX data port.

TABLE 164 - MAILBOX REGISTERS INTERFACE ACCESS PORTS

ACCESS PORT NAME	HOST ADDRESS	HOST TYPE	POWER PLANE	VCC2 POR	VCC1 POR
MBX INDEX	MBX Base Address	R/W	VCC2	0x00	-
MBX DATA	MBX Base Address + 1	R/W	VCC2	-	-

MAILBOX REGISTERS

There are 32 Mailbox Registers in the FDC37N972. The MBXA0–AF and MBX84– 91 Mailbox Registers are general purpose registers. There are no interrupts for these registers.

THE SYSTEM/8051 INTERFACE REGISTERS`

Mailbox Register 0, System-to-8051, and Mailbox Register 1, 8051-to-System, are specifically designed to pass commands between the host and the 8051 (FIGURE 35). If enabled, these registers can generate interrupts.

Mailbox Register 0 and Mailbox Register 1 are not dual-ported, so the System BIOS and Keyboard BIOS must be designed to properly share these registers. When the host performs a write of the System-to-8051 mailbox register, an 8051 INT1 will be generated and seen by the 8051 if unmasked. When the 8051 writes to the System-to-8051 mailbox register, the data is blocked but the write forces the register to 0x00, providing a simple means for the 8051 to inform that host that an operation has been completed.

When the 8051 writes the 8051-to-System mailbox register, an SMI may be generated and seen by the host if unmasked. When the Host CPU writes to the 8051-to-System mailbox register, the data is blocked but the write forces the 8051-to-System register to clear to zero, providing a simple means for the host to inform that 8051 that an operation has been completed.

PROGRAMMER'S NOTE: The protocol used to pass commands back and forth through the Mailbox Registers Interface is left to the system designer. SMSC can provide an application example of working code in which the host uses the Mailbox registers to gain access to all of the 8051 registers.

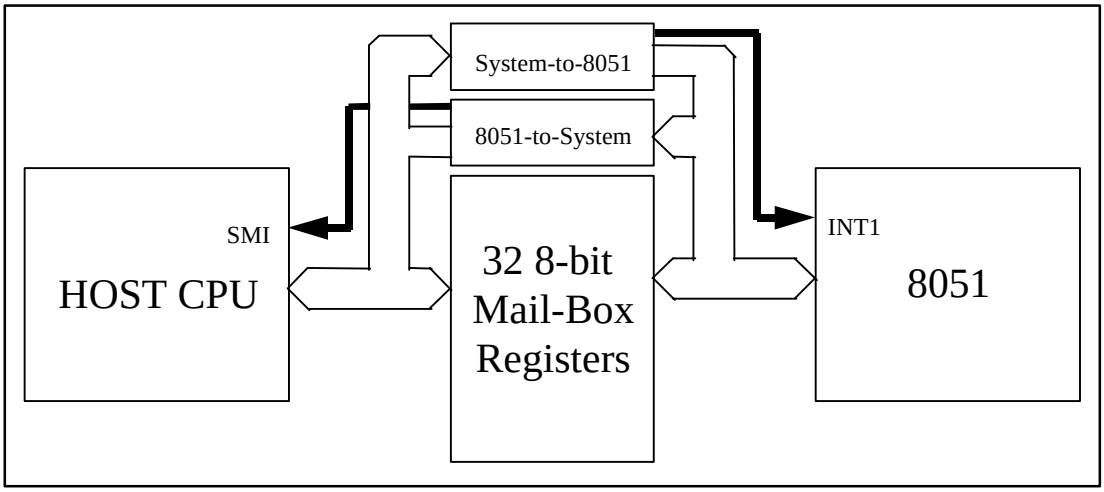


FIGURE 35 - SYSTEM-TO-8051 MAILBOX INTERFACE REGISTERS BLOCK DIAGRAM

Mailbox Register 0: System-to-8051

If enabled, an INT1 will be generated when the System writes to Mailbox Register 0 (TABLE 165). The interrupt source bit will be cleared when the 8051 reads this register.

After reading Mailbox Register 0, the 8051 can clear the register to "00H" by a dummy write to inform the host that the register contents have been read.

TABLE 165 - MAILBOX REGISTER 0 (SYSTEM-TO-8051)

MAILBOX INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
0x82	0x7F08	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE[1]	**RC**	**RC**	**RC**	**RC**	**RC**	**RC**	**RC**	**RC**
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0

NOTE[1] **RC** = Read-only register is cleared when written.

Mailbox Register 1: 8051-to-system

If enabled, an SMI will be generated when the 8051 writes to Mailbox Register 1 (TABLE 166). The SMI interrupt will be cleared when the host reads this register.

After reading Mailbox Register 1, the system can clear the register to “00H” by a dummy write to inform the 8051 that the register has been read.

TABLE 166 - MAILBOX REGISTER 1 (8051-TO-SYSTEM)

MAILBOX INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
0x83	0x7F09	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE[1]	**RC**	**RC**	**RC**	**RC**	**RC**	**RC**	**RC**	**RC**
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	D7	D6	D5	D4	D3	D2	D1	D0

NOTE[1] **RC** = Read-only register is cleared when written.

LED CONTROLS

The FDC37N972 has three independent LED outputs that are programmable under 8051 control.

LED REGISTER

Host	N/A
8051	0x7F21
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Default	0	0	0	N/A	0	0	0	0
8051 access	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W
Bit def	FDD Led Enable	FDD_ LED1	FDD_ LED0	Status of pin MODE	PWR_ LED1	PWR_ LED0	BAT_ LED1	BAT_ LED0
	Note 1	00 FDD LED is off 01 LED flash; P=1.0 sec 10 LED flash; P=0.5 sec 11 LED is fully on			00 PWR LED is off 01 LED flash; P=3.0 sec 10 LED flash; P=1.5 sec 11 LED is fully on		00 Battery LED is off 01 LED flash; P=1.0 sec 10 LED flash; P=0.5 sec 11 LED is fully on	

Note 1: D7 =1; FDD_LED Pin is controlled by D6, D5, D7=0; FDD_LED is controlled by the Motor Enable 0 pin from the FDC. When Motor Enable 0 pin is asserted the LED is on.

LED on time is T=125msec; “0” is on, “1” is off. Period “P” is indicated above.

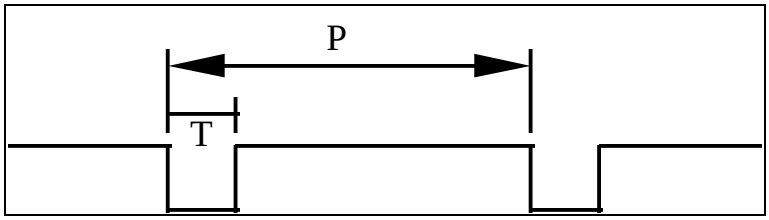


FIGURE 36 - LED OUTPUT

PULSE WIDTH MODULATORS

OVERVIEW

In the FDC37N972 there are two independent programmable Pulse-Width Modulated Fan Speed Controllers. The FDC37N972 PWM Fan Speed Controllers each include 11 fan speeds (F_{OUT}), 6-bit pulse-width resolution, and the ability to force the PWM outputs always high or low (**TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = "0")**. **NOTE**: each PWM Fan Speed Controller in the FDC37N972 has two fan speeds, 7-bit pulse-width resolution, and can only force the PWM output always low (when DCC = 0).

The FDC37N972 PWM Fan Speed Controllers can be driven by the system clock when VCC2 is active, or by the 32.768kHz standby clock (RTC) that is available when either VCC2 or VCC1 are active.

PROGRAMMER'S NOTE: the availability of the 32kHz standby clock is subject to the affects of the RTC clock control bits.

The PWM Fan Speed Control and Fan Control registers are accessible to both the Host and the 8051 through the Mailbox register interface (see MAILBOX REGISTER INTERFACE on page 249).

TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = "0")

FANx STDBY CLOCK BIT[5]	FANx CLOCK CONTROL BIT[1]	FANx CLOCK MULTI-PLIER BIT[2]	FANx CLOCK SELECT 1 BIT[3]	FANx CLOCK SELECT 0 BIT[4]	F_{OUT}[6] (kHz)	6-BIT DUTY CYCLE CONTROL (DCC)	DUTY CYCLE (%)
0	0	X	X	X	0 (low)	0	-
0	0	0	0	0	15.625	1-63	(DCC ÷ 64) × 100
0	0	0	0	1	23.438		
0	0	0	1	0	.040		
0	0	0	1	1	.060		
0	0	1	0	0	31.25		
0	0	1	0	1	46.876		
0	0	1	1	0	.080		
0	0	1	1	1	.120		
0	1	X	X	X	0 (high)	-	-

TABLE 168 – FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = "1")

FANx STDBY CLOCK BIT[5]	FANx CLOCK CONTROL BIT[1]	FANx CLOCK MULTI-PLIER BIT[2]	FANx CLOCK SELECT 1 BIT[3]	FANx CLOCK SELECT 0 BIT[4]	F_{OUT}[6] (kHz)	6-BIT DUTY CYCLE CONTROL (DCC)	DUTY CYCLE (%)
1	0	X	X	X	0 (low)	0	-
1	0	X	0	0	.032	1-63	(DCC ÷ 64) × 100
1	0	X	0	1	.064		
1	0	X	1	0	.128		
1	0	X	1	1	RESERVED		
1	1	X	X	X	0 (high)	-	-

NOTE[1] This is Fan Speed Control register bit 0
NOTE[2] This is Fan Control register Bit 2 or Bit 3
NOTE[3] This is Fan Control register Bit 0 or Bit 1
NOTE[4] This is Fan Speed Control register Bit 7
NOTE[5] This is Fan Control register Bit 4 or Bit 5
NOTE[6] The F_{OUT} frequency tolerance is 5%

There are two Fan Speed Control registers: PWM0 and PWM1. Both of these registers are located in the FDC37N972 Mailbox Registers Interface. PWM0 is MBX92 and PWM1 is MBX93 (see MAILBOX REGISTER INTERFACE on page 249).

The Fan Speed Control registers are in the FDC37N972 as shown in TABLE 169 and TABLE 170.

The default values for both the PWM0 and the PWM1 registers are 0x00. These defaults take effect on VCC1 POR.

TABLE 169 - FAN 1 SPEED CONTROL REGISTER (PWM0)

MAILBOX INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
0x92	0x7F25	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	FAN CLOCK SELECT 0	DUTY CYCLE CONTROL						FAN CLOCK CONTROL

TABLE 170 – FAN 2 SPEED CONTROL REGISTER (PWM1)

MAILBOX INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
0x93	0x7F26	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	FAN CLOCK SELECT 0	DUTY CYCLE CONTROL						FAN CLOCK CONTROL

FAN CLOCK SELECT 0, D7

The Fan Clock Select 0 bit D7 in the Fan Speed Control registers is used with the Fan Clock Select 1 and the Fan Clock Multiplier bits in the Fan Control register to determine the fan speed F_{OUT}.

NOTE: there are separate PWM0 and PWM1 Fan Clock Select 1 and Fan Clock Multiplier bits in the Fan Control register (see Section 0 Fan Control Register).
The affects of the Fan Clock Select[1:0] bits are shown TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”) and in TABLE 168 – FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “1”).

DUTY CYCLE CONTROL, D6 – D1

The Duty Cycle Control (DCC) bits determine the PWM fan duty cycle. The FDC37N972 has ≈1.56% duty cycle resolution.

When DCC = “000000” (min. value), F_{OUT} is always low. When DCC is “111111” (max. value), F_{OUT} is almost always high; i.e., high for $63/64^{th}$ and low for $1/64^{th}$ of the F_{OUT} period.

Generally, the F_{OUT} duty cycle (%) is (DCC ÷ 64) × 100.

Fan Clock Control, D0

The Fan Clock Control bit D0 is used to override the Duty Cycle Control bits and force F_{OUT} always high.

When D0 = "0", the DCC bits determine the F_{OUT} duty cycle. When D0 = 1, F_{OUT} is always high, regardless of the state of the DCC bits.

Fan Control Register

The Fan Control register contains Fan Clock Select 1, Fan Clock Multiplier, and Standby Clock control bits for each of the two Fan Speed Controllers PWM0 and PWM1.

The Fan Control register is MBX9D register (See Mailbox Registers Interface (TABLE 171)). The default value for the Fan Control Register is 0x30. The default value takes effect on VCC1 POR.

RESERVED bits in the Fan Control Register cannot be written and return "0" when read.

TABLE 171 - FAN CONTROL REGISTER

MAILBOX INDEX	8051 ADDRESS	POWER PLANE	DEFAULT
0x9D	0x7F28	VCC1	0x30

	D7	D6	D5	D4	D3	D2	D1	D0
MBX TYPE	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
8051 TYPE	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RESERVED		FAN2 (PWM1) STDBY CLOCK[1]	FAN1 (PWM0) STDBY CLOCK[1]	FAN2 (PWM1) CLOCK MULTI-PLIER	FAN1 (PWM0) CLOCK MULTI-PLIER	FAN2 (PWM1) CLOCK SELECT 1	FAN1 (PWM0) CLOCK SELECT 1

NOTE[1]: The FANx STDBY CLOCK bits, D4 and D5, should not be switched when PWRGD is inactive; i.e., when VCC2 = 0V.

FAN2 (PWM1) STDBY CLOCK, D5

The FAN2 (PWM1) STDBY CLOCK bit D5 is used to determine the Fan2 controller clock source.

When the FAN2 STDBY CLOCK bit = “1”, the Fan2 controller clock source is the 32.768kHz RTC clock (VCC1/VCC2). The available Fan2 F_{OUT} frequencies when D5 = “1” are shown in **TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”)**.

When the FAN2 STDBY CLOCK bit = “0”, the Fan2 controller clock source is the system clock (VCC2). The available Fan2 F_{OUT} frequencies when D5 = “0” are shown in **TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”)**.

The FAN2 (PWM1) STDBY CLOCK bit default = “1”.

FAN1 (PWM0) STDBY CLOCK, D4

The FAN1 (PWM0) STDBY CLOCK bit D4 is used to determine the Fan1 controller clock source.

When the FAN1 STDBY CLOCK bit = “1”, the Fan1 controller clock source is the 32.768kHz RTC clock (VCC1/VCC2). The available Fan1 F_{OUT} frequencies when D4 = “1” are shown in **TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”)**.

When the FAN1 STDBY CLOCK bit = “0”, the Fan1 controller clock source is the system clock (VCC2). The available Fan1 F_{OUT} frequencies when D4 = “0” are shown in **TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”)**.

The FAN1 (PWM0) STDBY CLOCK bit default = “1”.

FAN2 (PWM1) CLOCK MULTIPLIER, D3

The FAN2 Clock Multiplier bit D3 is used with the FAN2 Clock Select 1 bit D1 and the PWM1 Clock Select 0 bit MBX93.7 to determine the FAN2 F_{OUT} when the FAN2 STDBY CLOCK select bit is “0”.

When the FAN2 Clock Multiplier bit = “0”, no clock multiplier is used. When the FAN2 Clock Multiplier bit = “1”, the clock speed determined by the FAN2 Clock Select [1:0] bits is doubled (**TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”)**).

The FAN2 Clock Multiplier bit does not affect the FAN2 F_{OUT} when the FAN2 STDBY CLOCK select bit is “1”. Fan1 (PWM0) Clock Multiplier, D2

The FAN1 Clock Multiplier bit D2 is used with the FAN1 Clock Select 1 bit D0 and the PWM0 Clock Select 0 bit MBX92.7 to determine the FAN1 F_{OUT} when the FAN1 STDBY CLOCK select bit is “0”.

When the FAN1 Clock Multiplier bit = “0”, no clock multiplier is used. When the FAN1 Clock Multiplier bit = “1”, the clock speed determined by the FAN1 Clock Select [1:0] bits is doubled (**TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = “0”)**).

The FAN1 Clock Multiplier bit does not affect the FAN1 F_{OUT} when the FAN1 STDBY CLOCK select bit is “1”.

FAN2 (PWM1) CLOCK SELECT 1, D1

The FAN2 Clock Select 1 bit D1 is used with the FAN2 Clock Multiplier bit D3 and the PWM1 Clock Select 0 bit MBX93.7 to determine the FAN2 F_{OUT}.

The affects of the Fan Clock Select [1:0] bits are shown in **TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = "0") and TABLE 168.**

FAN1 (PWM0) CLOCK SELECT 1, D0

The FAN1 Clock Select 1 bit D0 is used with the FAN1 Clock Multiplier bit D2 and the PWM0 Clock Select 0 bit MBX92.7 to determine the FAN1 F_{OUT} .

The affects of the Fan Clock Select [1:0] bits are shown in **TABLE 167 - FAN SPEED CONTROL SUMMARY (STDBY CLOCK BIT = "0")** and TABLE 168.

ESMI REGISTERS

The host cam enable/disable the SMI interrupts generated as a result of the 8051 writing to Mailbox register 1. The host can read the ESMI source register to determine fo the FDC37N972 Mailbox interface was the cause of the SMI.

TABLE 172 - ESMI SOURCE REGISTER

HOST ADDRESS	MBX96
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/W	R/	R/	R/
BIT NAME	Reserved	Res	Res	Res	8051_WR	Res	Res	Res

8051_WR

This bit is set when a 8051-to-host mailbox has been written. This bit is cleared by a read of Mailbox Register 1 (MBX83.)

TABLE 173 - ESMI MASK REGISTER

HOST ADDRESS	MBX97
8051 ADDRESS	N/A
POWER	VCC2
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R/W	R	R	R/
BIT NAME	Reserved	Res	Res	Res	ESMI_ MASK	Reserved	Reserved	Reserved

ESMI_MASK

Setting this bit masks the 8051-to-host mailbox SMI.

8051 CONTROLLED PARALLEL PORT

To facilitate activities such as reprogramming the Flash Memory without opening the unit, the 8051 is able to take control of the parallel port interface. The 8051 has three memory mapped registers that look like the host's standard parallel port registers (Status, Control, and Data) with one exception: the 8051's Parallel Port Status register contains a write bit (bit 0) that allows the 8051 to disconnect the interface from the host and take control. Refer to the Parallel Port section for more information.

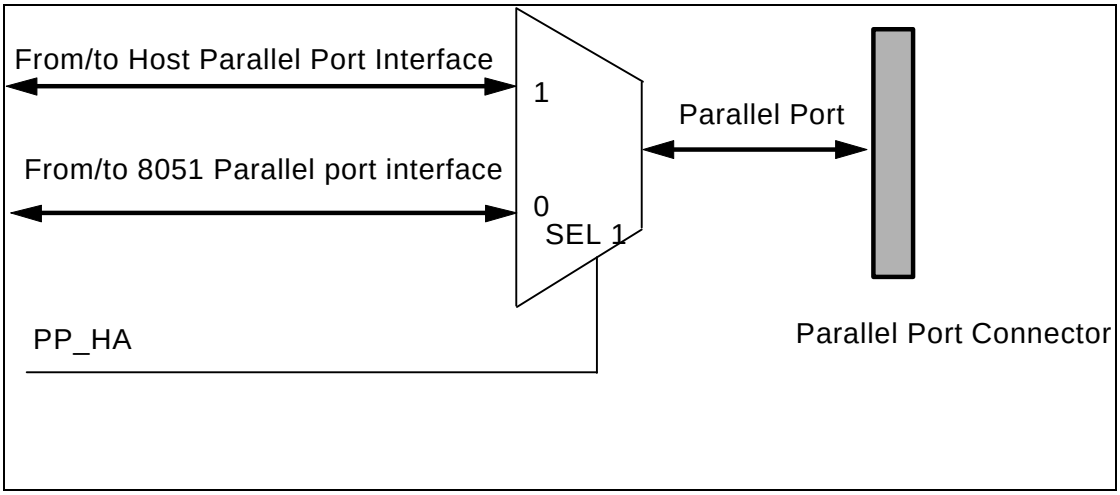


FIGURE 37 - PARALLEL PORT MULTIPLEXOR

OPERATION REGISTERS

The 8051 uses the following three memory mapped registers to gain access to and control the parallel port interface.

PARALLEL PORT STATUS REGISTER

Host	N/A
8051	0x7F3A
Power	VCC2
Default	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8051 R/W	R	R	R	R	R	R	R	R/W
System R/W	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Bit Def	nBUSY	nACK	PE	SLCT	nERR	0	0	PP_HA 1 = Host (or FDC) controls the Parallel Port Interface. 0 = 8051 controls the Parallel Port Interface (default).

If 8051 access to the parallel port pins is enabled; The level of the parallel port status pins can be read by reading this register.

Bit D7 (nBUSY): reflects the inverse state of pin BUSY
Bit D6 (nACK): reflects the current state of pin nACK
Bit D5 (PE): reflects the current state of pin PE
Bit D4 (SLCT): represents the current state of pin SLCT
Bit D3 (nERR): reflects the current state of pin nERR

PARALLEL PORT CONTROL REGISTER

Host	N/A
8051	0x7F3B
Power	VCC2
Default	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
System R/W	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Bit Def	0	0	PCD	0	SLCTIN	nINIT	ALF	STROBE

If 8051 access to the parallel port pins is enabled, the value of STROBE, ALF and SLCTIN are inverted and output onto the parallel port control pins. The value of nINIT is output onto the parallel port control pins. If PCD (Parallel Control Direction) = 0, the data bus is output. If PCD = 1 the parallel port data bus is floating to allow read data in.

PARALLEL PORT DATA REGISTER

Host	N/A
8051	0x7F3C
Power	VCC2
Default	0x00

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
8051 R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
System R/W	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Bit Def	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

If 8051 access to the parallel port pins is enabled; When read, this register reads the logic levels on the parallel port pins.

HOST CONTROLLED IR PORT

It is possible to give direct control of the IRRX and IRTX pins to the Host CPU by setting bit 2 of the Multiplexing_1 Register. The Host communicates to the pins through its memory mapped IR Data Register shown here.

IR DATA REGISTER

Host	MBX 0x98
8051	N/A
Power	VCC2
Default	0x00

	D7-D2	**D1**	**D0**
8051 R/W	N/A	N/A	N/A
System R/W	R/W	R	R/W
Bit Def	Reserved	IR_REC	IR_TX

Bit 1 and bit 0 are don't care if bit 2 of the Multiplexing_1 Register is reset. (These bits are multiplexed onto the IRTX and IRRX pins when bit 2 of the Multiplexing Register is set).

Therefore, if the IR interface is on IRRX (pin 21) and IRTX (pin 20), then MISC2 allows the IR interface to be switched between the IRCC 2.0 block and the IR Data Register.

Note that MISC7 allows the control of the COM-RX/GPIO8 (pin 141) and COM-TX/GPIO9 (pin 142) pins. If the COM-RX and COM-TX pins are used for IR, then this allows the IR interface access to be switched between the IRCC 2.0 block and the 8051.

GENERAL PURPOSE I/O (GPIO)

All General Purpose registers are powered by VCC1. When GPIO6, GPIO10, OUT1, OUT5 - OUT9, GPIO17, GPIO20, GPIO21, and KSO12 are configured as alternate function outputs and PWRGD is inactive, i.e. VCC2 is 0v, these pins will tri-state to prevent back-biasing of external circuitry.

- GPIO9 defaults to “output”, “low”, for both the default (GPIO) function and the alternate (IRTX) function, regardless of the state of PWRGD. This is done to prevent infrared transceiver damage

The GPIO defaults are shown in TABLE 86 - 8051 ON-CHIP EXTERNAL MEMORY MAPPED REGISTERS on page 159.

PROGRAMMER’S NOTE: The direction of alternate function pins that are multiplexed with general purpose I/O pins, i.e. where the GPIO function is the default, is determined by the GPIO direction bit. For example if the KS014 function of GPIO4 is selected, bit 4 in GPIO Direction Register A must be set to “1”. This rule does not apply to default non-GPIO pin functions that may have a GPIO as an alternate function.

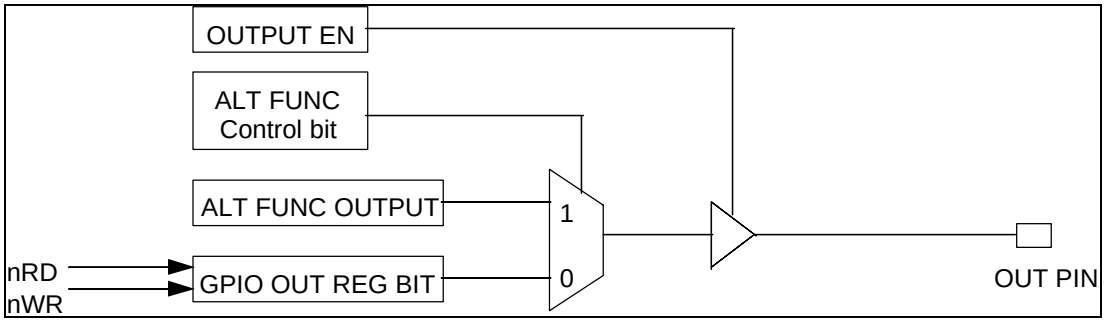


FIGURE 38 - OUTPUT PIN TYPE

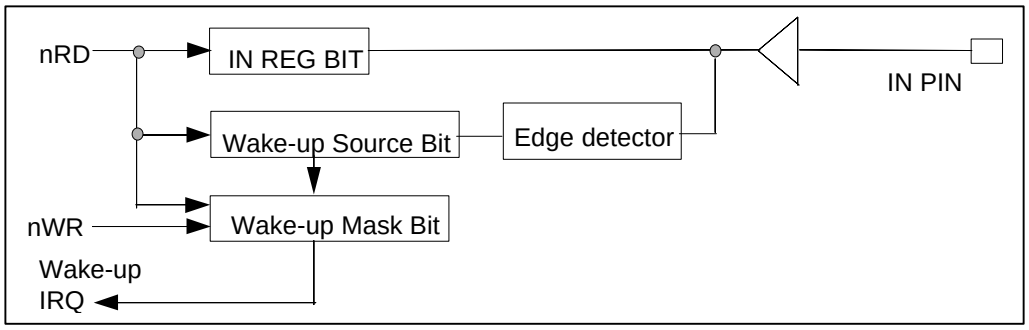


FIGURE 39 - INPUT PIN TYPE

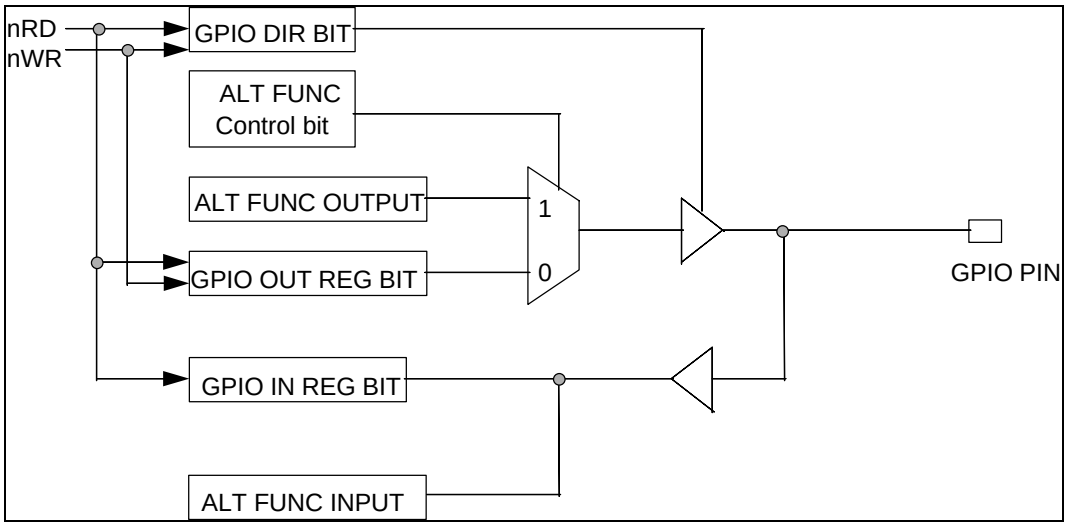


FIGURE 40 - GPIO PIN TYPE

MEMORY MAPPED CONTROL REGISTERS

GPIO DIRECTION REGISTER A

Host	N/A
8051	0x7F18
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def	GPIO7 1=output 0=input	GPIO6 1=out-put 0=input	GPIO5 1=out-put 0=input	GPIO4 1=out-put 0=input	GPIO3 1=out-put 0=input	GPIO2 1=out-put 0=input	GPIO1 1=out-put 0=input	GPIO0 1=out-put 0=input

GPIO INPUT REGISTER A

Host	N/A
8051	0x7F1A (R)
Power	VCC1
Default	N/A

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Des.	status of pin GPIO7	status of pin GPIO6	status of pin GPIO5	status of pin GPIO4	status of pin GPIO3	status of pin GPIO2	status of pin GPIO1	status of pin GPIO0

GPIO OUTPUT REGISTER A

Host	N/A
8051	0x7F19
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Des.	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

GPIO DIRECTION REGISTER B

Host	N/A
8051	0x7F1B
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	GPIO15 1=out-put 0=input	GPIO14 1=out-put 0=input	GPIO13 1=out-put 0=input	GPIO12 1=out-put 0=input	GPIO11 1=out-put 0=input	GPIO10 1=out-put 0=input	GPIO9 1=out-put 0=input	GPIO8 1=out-put 0=input

GPIO OUTPUT REGISTER B

1Host	N/A
8051	0x7F1C
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	GPIO 15	GPIO 14	GPIO 13	GPIO 12	GPIO 11	GPIO 10	GPIO 9	GPIO 8

GPIO INPUT REGISTER B

Host	N/A
8051	0x7F1D (R)
Power	VCC1
Default	N/A

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	status of pin GPIO15	status of pin GPIO14	status of pin GPIO13	status of pin GPIO12	status of pin GPIO11	status of pin GPIO10	status of pin GPIO9	status of pin GPIO8

GPIO DIRECTION REGISTER C

Host	N/A
8051	0x7F1E
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Des.	0	0	GPIO21 1=output 0=input	GPIO20 1=output 0=input	GPIO19 1=output 0=input	GPIO18 1=output 0=input	GPIO17 1=output 0=input	GPIO16 1=output 0=input

GPIO OUTPUT REGISTER C

Host	N/A
8051	0x7F1F
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	0	0	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16

GPIO INPUT REGISTER C

Host	N/A
8051	0x7F20 (R)
Power	VCC1
Default	N/A

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	0	0	status of pin GPIO21	status of pin GPIO20	status of pin GPIO19	status of pin GPIO18	status of pin GPIO17	status of pin GPIO16

OUT REGISTER D

Host	N/A
8051	0x7F22
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

OUT REGISTER E

Host	N/A
8051	0x7F23
Power	VCC1
Default	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	0	0	0	0	OUT11	OUT10	OUT9	OUT8

IN REGISTER F

Host	N/A
8051	0x7F24 (R)
Power	VCC1
Default	N/A

	D7	D6	D5	D4	D3	D2	D1	D0
Bit Def.	status of pin IN7	status of pin IN6	status of pin IN5	status of pin IN4	status of pin IN3	status of pin IN2	status of pin IN1	status of pin IN0

MULTIFUNCTION PIN

OVERVIEW

The FDC37N972 multifunction pins are mutliplexed on the following pins :

1. Multiplexing is required for nIRQ8.
2. PWM0 and PWM1 have independent multiplex controls.
3. Multiplexing is required for the Flash ROM address bit FA18.
4. Multiplexing is required for the Flash ROM chip select nFCS.
5. Multiplexing is required for the ACCESS.bus 2 interface pins AB2_DATA and AB2_CLK.
6. OUT0 can be an open-drain or push-pull driver.

Refer to **TABLE 4 - ALTERNATE FUNCTION PINS** on page 26 for a complete list of the FDC37N972 multifunction pins.

The 8051 firmware, alone, controls the multiplexing functions for each of the multiplexed pins described in this section.

MULTIPLEXING_1 REGISTER

TABLE 174 - MULTIPLEXING_1 REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F3D	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	**-**	**-**	**-**	**-**	**-**	**-**	**-**	**-**
8051 TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	MISC7	MISC6	MISC5	MISC4	MISC3	MISC2	MISC1	MISC0

MISC7 – D7

The MISC7 bit is used in the FDC37N972 to select the pin function and the buffer mode between GPIO8 – GPIO9 and IRRX and IRTX TABLE **175**.

TABLE 175 - MISC7 BIT

PIN	MISC7 = 0 (DEFAULT)	MISC7 = 1
GPIO8	GPIO8	IRCC BLOCK COM-RX PORT
GPIO9	GPIO9	IRCC BLOCK COM-TX PORT

MISC6 – D6

The MISC6 bit is used in the FDC37N972 to select the pin function and the buffer mode between GPIO17 and GATEA20 (TABLE **176**).

TABLE 176 - MISC6 BIT

PIN	MISC6 = 0 (DEFAULT)	MISC6 = 1
GPIO17	GPIO17	GATEA20

MISC5 – D5

The MISC5 bit is used in the FDC37N972 to select the pin function and the buffer mode between OUT5 and OUT6 and the FDC Floppy 1 drive controls nDS1 and nMTR1 (TABLE 177).

TABLE 177 - MISC5 BIT

PIN	MISC5 = 0 (DEFAULT)	MISC5 = 1
OUT5	OUT5	nDS1
OUT6	OUT6	nMTR1

MISC4 – D4

The MISC4 bit is used in the FDC37N972 to select the pin function and the buffer mode between OUT10 and PWM0 for the OUT10 pin (TABLE 178).

NOTE: This function only applies to the OUT10/PWM0 pin. The OUT11/PWM1 functions are selected by MISC12 (Multiplexing_2 Register, below).

NOTE: The MISC4 bit in the FDC37C95X applies to both OUT10/PWM0 and OUT11/PWM1.

TABLE 178 - MISC4 BIT

MISC4	DESCRIPTION
0	OUT10 Pin Function Selected (**DEFAULT**)
1	PWM0 Pin Function Selected

MISC3 – D3

The MISC3 bit, along with the MISC1 bit, is used in the FDC37N972 to select the pin function and the buffer mode between GPIO20 and GPIO21, the 8051 UART RX and TX, and the PS/2 CLK and DATA (TABLE 179).

TABLE 179 - MISC3 AND MISC1 BITS

MISC[3,1]	PIN GPIO20	PIN GPIO21
[0,0] (DEFAULT)	GPIO20 + 8051_RX *	GPIIO21
[0,1]	PS2CLK	PS2DAT
[1,0]	GPIO20 + 8051_RX *	8051_TX **
[1,1]	PS2CLK	PS2DAT

GPIO20_DIR bit should be set to 0 when operating as an 8051_RX pin.
** GPIO21_DIR bit must be set to 1 when operating as an 8051_TX pin.

The PS/2 pins on GPIO20 and GPIO21 are disabled (internally pulled high) when the non-PS/2 alternate functions are selected. The PS/2 inputs under this condition are seen as a high to the PS/2 Device Interface logic.

Whenever a PS/2 channel is not enabled, the input signals to that channel must be high. The FDC37N972 provides this through the use of weak pull-ups since the EM and KB channels share a common receive path and **THE IM AND PS2 CHANNELS ALSO SHARE A COMMON RECEIVE PATH.**

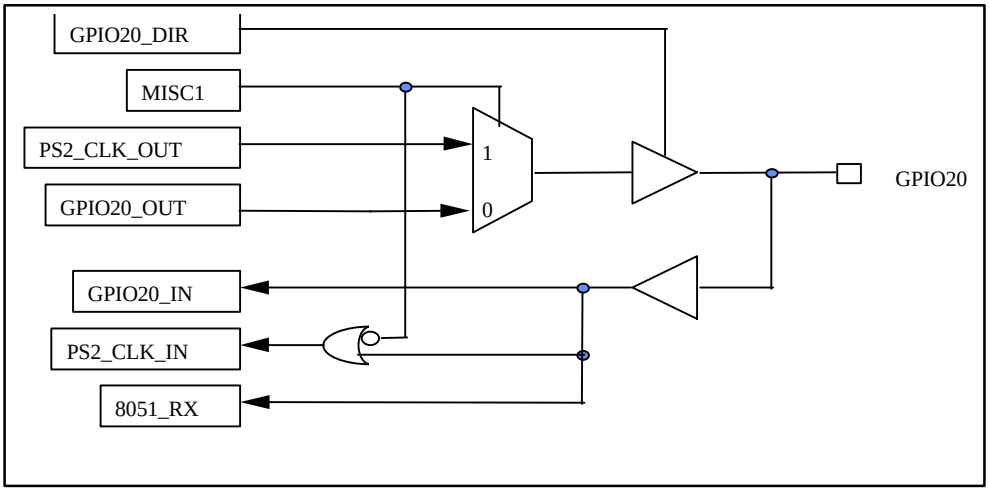


FIGURE 41 - GPIO20 ALTERNATE FUNCTION STRUCTURE

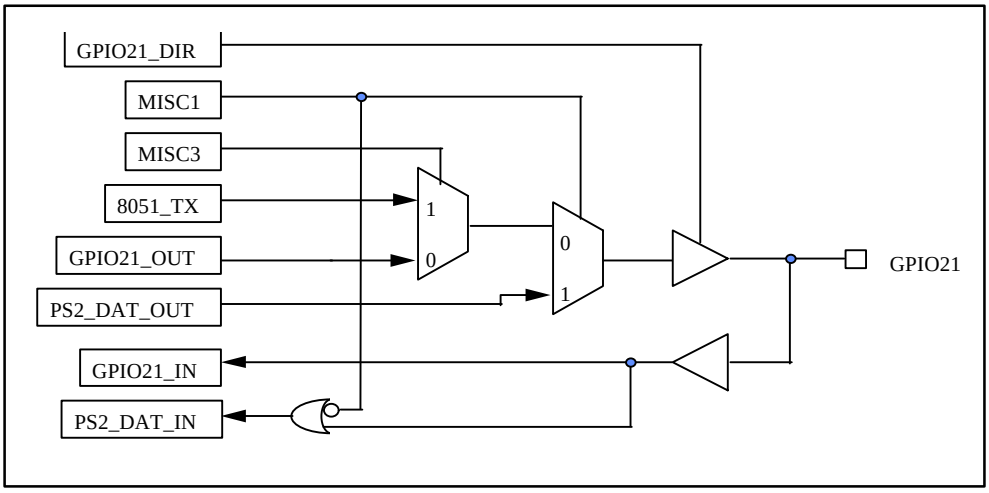


FIGURE 42 - GPIO21 ALTERNATE FUNCTION STRUCTURE

MISC2 – D2

TABLE 180 - MISC2 BIT

PIN	MISC2 = 0 (DEFAULT)	MISC2 = 1
IRTX	FROM IRCC BLOCK	FROM IR DATA REGISTER
IRRX	FROM IRCC BLOCK	FROM IR DATA REGISTER

MISC1 – D1

See the description of the MISC3 bit, above.

NOTE: the MISC1 bit is not used with the MISC0 bit in the FDC37N972.

MISC0 – D0

The MISC0 bit is used in the FDC37N972 to select the pin function and the buffer mode between OUT1 and nIRQ8 (TABLE 181).

TABLE 181 - MISC0 BIT

MISC0	DESCRIPTION
0	OUT1 Pin Function Selected (**DEFAULT**)
1	nIRQ8 Pin Function Selected

MULTIPLEXING_2 REGISTER

TABLE 182 - MULTIPLEXING_2 REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F40	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	MISC16	MISC15	MISC14	MISC13	MISC12	MISC11	MISC10	MISC9

MISC[16:15], D7 – D6

The function of the GPIO10 pin is RESERVED in the FDC37N972 when MISC[16:15] = 1,1 (TABLE 183).

NOTE: the FDC37N972 supports a single 16C550 UART interface.

TABLE 183 - MISC[16:15] BITS

MULTIPLEXING_2 REGISTER BITS[7:6]		SELECTED PIN FUNCTION	
MISC16	**MISC15**	**FDC37C95x**	**FDC37N972**
0	0	GPIO10 (DEFAULT)	GPIO10 (DEFAULT)
0	1	IR_MODE	IR_MODE
1	0	IRRX3	IRRX3
1	1	nRTS2	RESERVED

MISC[14:13], D5 – D4

The MISC14 and MISC13 bits are used in the FDC37N972 to select the pin function and the buffer mode between GPIO6 and the IrCC 2.0 IRMODE and IRRX3 functions (TABLE 184).

TABLE 184 - MISC14 AND MISC13 BITS

MISC[14:13]	PIN GPIO6
[0:0] (DEFAULT)	GPIO6
[0:1]	IR_MODE (IRCC 2.0 GP DATA) OUTPUT
[1:0]	IRRX3 INPUT
[1:1]	RESERVED

MISC12 – D3
The MISC12 bit in the Multiplexing_2 register is used in the FDC37N972 to select the pin function and buffer mode between OUT11 and PWM1 for the OUT11 pin (TABLE 185).

NOTE: The MISC12 bit in the FDC37C95X selects between GPIO functions and Serial Port 2. The FDC37N972 supports a single 16C550 UART interface.

TABLE 185 - MISC12 BIT

MISC12	DESCRIPTION
0	OUT11 Pin Function Selected (**DEFAULT**)
1	PWM1 Pin Function Selected

MISC11

The MISC11 bit is used in the FDC37N972 to select the pin function and the buffer mode between GPIO19, OUT9 and DMA Channel 3 (TABLE 186).

TABLE 186 - MISC11 BIT

MISC11	PIN OUT9	PIN GPIO19
0 (DEFAULT)	OUT9	GPIO19
1	DRQ3	nDACK3

MISC10

TABLE 187 - MISC10, MISC17, AND MISC6 BITS

MISC17	MISC10	MISC6	PIN OUT8	PIN KSO12
0	0	0	OUT8	KSO12
0	0	1	CPU_RESET	KSO12
0	1	X	DRQ2	KSO12
1	0	0	OUT8	OUT8
1	0	1	CPU_RESET	CPU_RESET
1	1	0	DRQ2	OUT8
1	1	1	DRQ2	CPU_RESET

With this definition, only the pair [OUT8 & CPU_RESET] can not simultaneously exist on pins OUT8 and KS012.

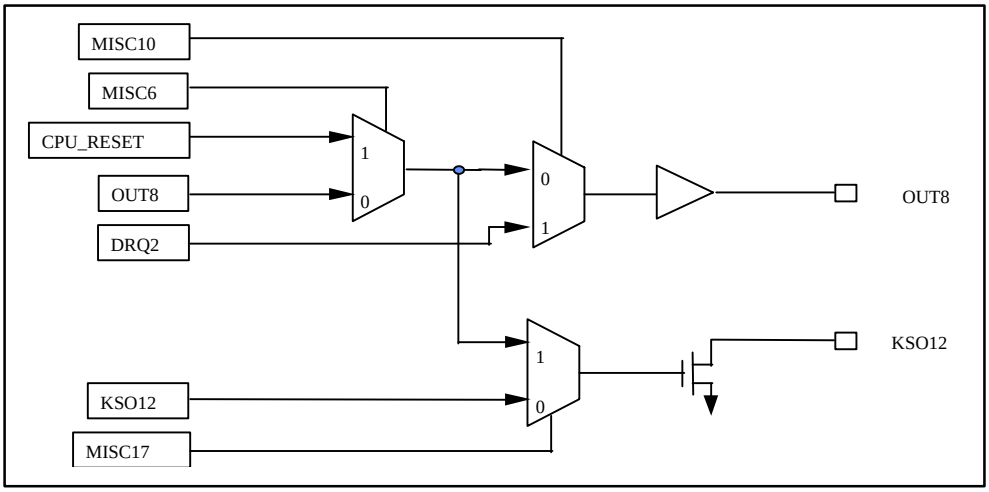


FIGURE 43 - OUT8 AND KSO12 ALTERNATE FUNCTION OPERATION

MISC9

TABLE 188 - MISC9 BIT

MISC9	PIN GPIO4	GPIO5
0 (DEFAULT)	GPIO4	GPIO5
1	KSO14	KSO15

MULTIPLEXING_3 REGISTER

TABLE 189 - MULTIPLEXING_3 REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F30	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	MISC23	MISC22	MISC21	MISC20	MISC19	MISC18	MISC17	MISC8

MISC23 – D7

The buffer type for the GPIO7 pin can be programmed as push-pull or open-drain. This makes GPIO7 useful for other unique functions like nSCI and extended keyboard scan controls like KSO16. The

MISC23 bit is used in the FDC37N972 to select the buffer mode for the GPIO7 pin (**TABLE 190 - MISC23 BIT**).

TABLE 190 - MISC23 BIT

MISC23	DESCRIPTION
0	Buffer Mode for GPIO7 is Push-Pull (**DEFAULT**)
1	Buffer Mode for GPIO7 is Open-Drain

MISC22 – D6

The MISC22 bit is used along with the MISC5 bit in Multiplexing_1 register to select the KBRST alternate function #2 of the OUT5 pin (Table 191 - MISC22 BIT).

TABLE 191 - MISC22 BIT

MISC5	MISC22	DESCRIPTION
1	X	nDS1 Pin Function Selected.
0	0	OUT5 Pin Function Selected (**DEFAULT**)
0	1	KBRST Pin Function Selected

MISC21 – D5

The MISC21 bit is used in the FDC37N972 to select the buffer mode for the OUT0 pin (TABLE 192).

TABLE 192 - MISC21 BIT

MISC21	DESCRIPTION
0	Buffer Mode for OUT0 is Open-Drain (**DEFAULT**)
1	Buffer Mode for OUT0 is Push-Pull

MISC20 – D4

The MISC20 bit in the Multiplexing_3 register is used in the FDC37N972 to select the pin function and buffer mode between GPIO and ACCESS.bus 2 functions for the GPIO11 and GPIO12 pins (TABLE 193).

TABLE 193 - MISC20 BIT

MISC20	DESCRIPTION
0	GPIO Pin Functions Selected (**DEFAULT**)
1	ACCESS.bus 2 Pin Functions Selected

MISC19 – D3

The MISC19 bit in the Multiplexing_3 register is used in the FDC37N972 to select the pin function and buffer mode between nFCS and GPIO0 for the nFCS pin (TABLE 194).

TABLE 194 - MISC19 BIT

MISC19	DESCRIPTION
0	nFCS Pin Function Selected (**DEFAULT**)
1	GPIO0 Pin Function Selected

MISC18 – D2

The MISC18 bit in the Multiplexing_3 register is used in the FDC37N972, along with bit D3 in the ES**MI MASK** register, to select the pin function and buffer mode for the OUT7 pin and the SMI transfer mechanism to the host. (TABLE 195).

When MISC18 = '0', the primary function of the OUT7 pin is selected and the SMI is routed to the Serial IRQ interface. If the SMI is masked, SIRQ slot3 is available as IRQ2.

When MISC18 = '1', the alternate nSMI function of the OUT7 pin is selected, the pad is driven open-drain, and the Serial IRQ slot3 is available as IRQ2.

TABLE 195 - MISC18 AND ESMI MASK BITS

ESMI MASK REGISTER[1]		FUNCTION		
D3	MISC18	OUT7 PIN	SIRQ SLOT3	DESCRIPTION
0	0	OUT7	nSMI	SERIAL SMI (**DEFAULT**)
0	1	nSMI	IRQ2	PARALLEL SMI, SERIAL IRQ IRQ2 AVAILABLE
1	0	OUT7	IRQ2	MASKED SERIAL SMI, IRQ2 AVAILABLE
1	1	nSMI	IRQ2	PARALLEL SMI MASKED (INACTIVE), IRQ2 AVAILABLE

NOTE[1] The ESMI Mask register is MBX97h (TABLE 162).

MISC17 – D1

TABLE 196 - MISC17

MISC17	PIN GPIO18	PIN KSO13
0	GPIO18 + nDACK2 (1)	KSO13
1	nDACK2	GPIO18

NOTE 1: nDACK2 can be received on the GPIO18 pin when MISC17 = 0 by setting the GPIO18 Direction bit to 0.

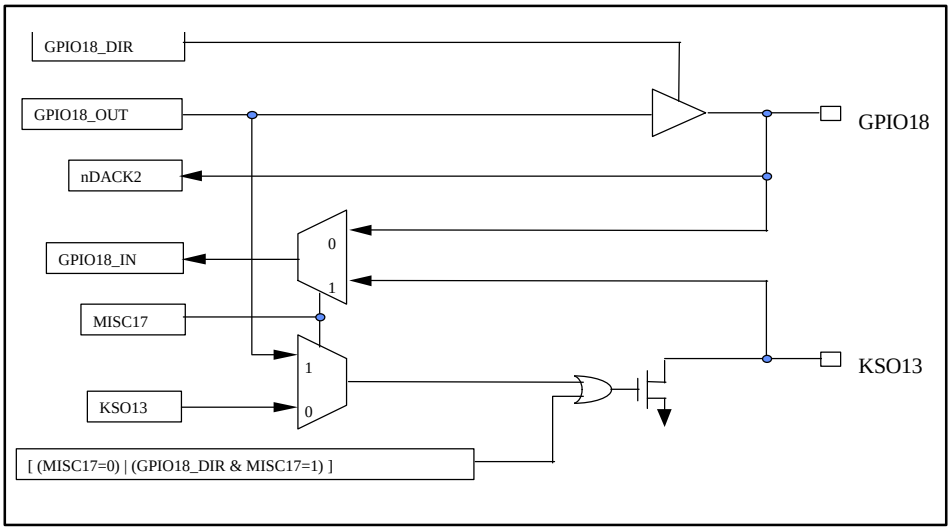


FIGURE 44 - GPIO18 AND KSO13 ALTERNATE FUNCTION OPERATION

MISC8 – D0

The MISC8 bit in the Multiplexing_3 register is used in the FDC37N972 to select the pin function and buffer mode between FA18 and GPIO13 for the FA18 pin (TABLE 197).

NOTE: The MISC8 bit in the FDC37C95X selects between the GPIO16 function and MID1. The FDC37N972 does not support the Media ID pins (see MID[1:0] FDD INTERFACE PINS on page 37).

TABLE 197 - MISC8 BIT

MISC8	DESCRIPTION
0	FA18 Pin Function Selected (**DEFAULT**)
1	GPIO13 Pin Function Selected

MISC8	PIN GPIO[16]
0 (default)	GPIO[16]
1	MID1

MISC17 is described in the Multiplexing_2 register section.

ACPI PM1 BLOCK

ACPI PM1 BLOCK OVERVIEW

The FDC37N972 supports ACPI as described in this section. These features comply with the ACPI Specification, Revision 1.0, through a combination of hardware and 8051 software.

The FDC37N972 implements the ACPI fixed registers but includes only those bits that apply to the power button sleep button and RTC alarm events. The ACPI WAK_STS, SLP_TYPx, and SLP_EN bits are also supported.

The registers in the FDC37N972 ACPI PM1 Block occupy eight addresses in the host I/O space and are specified as offsets from the ACPI PM1 Block base address. The ACPI PM1 Block base address is relocatable depending on the values programmed in FDC37N972 configuration registers CR60 and CR61 in Logical Device Number 1.

The functions described in the following sub-sections can generate a SCI event on the nEC_SCI pin. In the FDC37N972, an SCI event is considered the same as an ACPI wakeup or runtime event. The 8051 can also generate a SCI on the nEC_SCI pin by setting the 8051_SCI_STS bit in the 8051_PM_STS register (see nEC_SCI INTERFACE on page 287).

ACPI PM1 BLOCK SCI EVENT-GENERATING FUNCTIONS

Power Button With Override

The power button has a status and an enable bit in the PM1_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writeable by the 8051; the enable bit is Read-only by the 8051. It also has a status and enable bit in the PM1_BLK of registers to indicate and control the power button override (fail-safe) event. These bits are not required by ACPI. The power button override event status bit is software Read/Writeable by the 8051; the enable bit is software read-only by the 8051. The enable bit for the override event is located at bit 1 in the PM1_CNTRL2 register.

The power button enable bit is set by the Host to enable the generation of an SCI due to the power button event. The status bit is set by the 8051 when it generates a power button event and is cleared by the Host writing a ‘1’ to this bit (writing a ‘0’ has no effect); it can also be cleared by the 8051. If the enable bit is set, the 8051 will generate an SCI power management event.

Sleep Button

The sleep button has a status and an enable bit in the PM1_BLK of registers to provide an SCI upon the button press. The status bit is software Read/Writeable by the 8051; the enable bit is Read-only by the 8051.

The sleep button enable bit is set by the Host to enable the generation of an SCI due to the sleep button event. The status bit is set by the 8051 when it generates a sleep button event and is cleared by the Host writing a ‘1’ to this bit (writing a ‘0’ has no effect); it can also be cleared by the 8051. If the enable bit is set, the 8051 will generate an SCI power management event.

RTC Alarm

The ACPI specification requires that the RTC alarm generate a hardware wake-up event from the sleeping state. The RTC alarm can be enabled as an SCI event and its status can be determined through bits in the PM1_BLK of registers. The status bit is software

Read/Writeable by the 8051; the enable bit is Read-only by the 8051.

The RTC enable bit is set by the Host to enable the generation of an SCI due to the RTC alarm event. The status bit is set by the 8051 when the RTC generates an alarm event and is cleared by the Host writing a '1' to this bit (writing a '0' has no effect); it can also be cleared by the 8051. If the enable bit is set, the 8051 will generate an SCI power management event.

ACPI PM1 BLOCK BASE ADDRESS

Logical Device 1 in the FDC37N972 configuration space supports the ACPI PM1 Block registers interface.

Three device configuration registers in LDN1 provide activation control and the base address programming for the ACPI PM1 Block registers (TABLE 198).

Register 0x30 is the Activate register. The activation control (LDN1:CR30.0) qualifies address decoding for the ACPI PM1 Block registers; e.g., if the Activate bit D0 in the Activate register is "0", the PM1 Block addresses will not be decoded; if the Activate bit is "1", PM1 Block addresses will be decoded depending on the values programmed in the ACPI PM1 Block Primary Base Address registers.

Registers 0x60 and 0x61 are the ACPI PM1 Block Primary Base Address registers. Register 0x60 is the ACPI PM1 Block Primary Base Address High Byte, register 0x61 is the ACPI PM1 Block Primary Base Address Low Byte.

NOTE: The ACPI PM1 Block base address must be located on eight -byte boundaries; i.e., bits D0 – D2 in the ACPI PM1 Block Primary Base Address Low Byte must be "0". Valid ACPI PM1 Block base address values are 0x0000 – 0x0FF8.

TABLE 198 – ACPI PM1 BOCK CONFIGURATION REGISTERS (LDN1)

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1&VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							
						RESERVED							Activate
0x60	R/W	0x00	0x00	0x00	-	ACPI PM1 Block Primary Base Address High Byte							
						"0"	"0"	"0"	"0"	A11	A10	A9	A8
0x61	R/W	0x00	0x00	0x00	-	ACPI PM1 Block Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	"0"	"0"	"0"

ACPI PM1 BLOCK

DESCRIPTION

The ACPI register model consists of a number of fixed register blocks that perform designated functions. A register block consists of a number of registers that perform Status, Enable and Control functions. The ACPI specification deals with events (which have an associated interrupt status and enable bits, and sometimes an associated control function) and control features. The status registers illustrate what defined function is requesting ACPI interrupt services (SCI). Any status bit in the ACPI specification has the following attributes:

Status bits are only set through some defined hardware or 8051 event.
Unless otherwise noted, Status bits are cleared by the system writing a “1” to that bit position, and upon VCC1 POR. Writing a ‘0’ has no effect.

Status bits only generate interrupts while their associated bit in the enable register is set. Function bit positions in the status register have the same bit position in the enable register (there are exceptions to this rule, special status bits have no enables).

Note that this implies that if the respective enable bit is reset and the hardware event occurs, the respective status bit is set; however no interrupt is generated until the enable bit is set. This allows software to test the state of the event (by examining the status bit) without necessarily generating an interrupt. There are a special class of status bits that have no respective enable bit, these are called out specifically, and the respective enable bit in the enable register is marked as reserved for these special cases.

The enable registers allow the setting of the status bit to generate an interrupt (under 8051 control). As a general rule there is an enable bit in the enable register for every status bit in the status register. The control register provides special controls for the associated event, or special control features that are not associated with an interrupt event. The order of a register block is the status registers, followed by enable registers, followed by control registers.

REGISTERS

The registers in the FDC37N972 ACPI PM1 Block occupy eight addresses in the host I/O space and are specified as offsets from the ACPI PM1 Block base address (TABLE 199).

The registers in the PM1 Block are powered by VCC1.

TABLE 199 - ACPI PM1 BLOCK REGISTERS

REGISTER	SIZE (bits)	OFFSET	ADDRESS
PM1_STS 1	8	0	<ACPI PM1 Block Base Address>
PM1_STS 2	8	1	<ACPI PM1 Block Base Address>+1h
PM1_EN 1	8	2	<ACPI PM1 Block Base Address>+2h
PM1_EN 2	8	3	<ACPI PM1 Block Base Address>+3h
PM1_CNTRL 1	8	4	<ACPI PM1 Block Base Address>+4h
PM1_CNTRL 2	8	5	<ACPI PM1 Block Base Address>+5h
RESERVED	8	6	<ACPI PM1 Block Base Address>+6h
RESERVED	8	7	<ACPI PM1 Block Base Address>+7h

POWER MANAGEMENT 1 STATUS REGISTER 1 (PM1_STS 1)

Host Register Location: <ACPI PM1 Block Base Address> System I/O Space
8051 Register Location: n/a
Default Value: 00h on VCC1 POR
Host Attribute: Read
Size: 8-bits

BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return a value of zero.

POWER MANAGEMENT 1 STATUS REGISTER 2 (PM1_STS 2)

Host Register Location: <ACPI PM1 Block Base Address>+1h System I/O Space
8051 Register Location: 0x7F80
Default Value: 00h on VCC1 POR
Host Attribute: Read/Write (Note 1)
8051 Attribute Read/Write
Size: 8-bits

Note 1: These bits are set/cleared by the 8051 directly i.e., writing ‘1’ sets the bit and writing ‘0’ clears it. These bits can also be cleared by the Host software writing a one to this bit position and by VCC1 POR. Writing a 0 by the Host has no effect.

An interrupt is generated to the 8051 when the Host writes to this register.

BIT	NAME	DESCRIPTION
0	PWRBTN_STS	This bit can be set or cleared by the 8051 to simulate a Power button status if the power is controlled by the 8051. The Host writing a one to this bit can also clear this bit. The 8051 must generate the associated SCI interrupt under software control.

BIT	NAME	DESCRIPTION
1	SLPBTN_STS	This bit can be set or cleared by the 8051 to simulate a Sleep button status if the sleep state is controlled by the 8051. The Host writing a one to this bit can also clear this bit.
2	RTC_STS	This bit can be set or cleared by the 8051 to simulate a RTC status. The Host writing a one to this bit can also clear this bit.
3	PWRBTNOR_STS	This bit can be set or cleared by the 8051 to simulate a Power button override event status if the power is controlled by the 8051. The Host writing a one to this bit can also clear this bit.
4-6	Reserved	Reserved. These bits always return a value of zero.
7	WAK_STS	This bit can be set or cleared by the 8051. The Host writing a one to this bit can also clear this bit.

POWER MANAGEMENT 1 ENABLE REGISTER 1 (PM1_EN 1)

Host Register Location: <ACPI PM1 Block Base Address>+2 System I/O Space
8051 Register Location: n/a
Default Value: 00h on VCC1 POR
Host Attribute: Read
Size: 8-bits

BIT	NAME	DESCRIPTION
0-7	Reserved	Reserved. These bits always return a value of zero.

POWER MANAGEMENT 1 ENABLE REGISTER 2 (PM1_EN 2)

Host Register Location: <ACPI PM1 Block Base Address>+3 System I/O Space
8051 Register Location: 0x7F81
Default Value: 00h on VCC1 POR
Host Attribute: Read/Write
8051 Attribute: Read
Size: 8-bits

An interrupt is generated to the 8051 when the Host writes this to register.

BIT	NAME	DESCRIPTION
0	PWRBTN_EN	This bit can be read or written by the Host. It can be read by the 8051
1	SLPBTN_EN	This bit can be read or written by the Host. It can be read by the 8051
2	RTC_EN	This bit can be read or written by the Host. It can be read by the 8051
3-7	RESERVED	RESERVED bits cannot be written and return “0” when read.

POWER MANAGEMENT 1 CONTROL REGISTER 1 (PM1_CNTRL 1)

Host Register Location: <ACPI PM1 Block Base Address>+4 System I/O Space
8051 Register Location: n/a
Default Value: 00h on VCC1 POR
Host Attribute: Read
Size: 8-bits

BIT	NAME	DESCRIPTION
0-7	RESERVED	RESERVED bits cannot be written and return “0” when read.

POWER MANAGEMENT 1 CONTROL REGISTER 2 (PM1_CNTRL 2)

Host Register Location: <ACPI PM1 Block Base Address>+5 System I/O Space
8051 Register Location: 0x7F82
Default Value: 00h on VCC1 POR
Host Attribute: Read/Write
8051 Attribute: Read. **NOTE:** Bit 5 is Read/Write
Size: 8-bits

An interrupt is generated to the 8051 when the Host writes to this register.

BIT	NAME	DESCRIPTION
0	Reserved	Reserved. This field always returns zero.
1	PWRBTNOR_EN	This bit can be set or cleared by the Host, read by the 8051
2-4	SLP_TYPx	These bits can be set or cleared by the Host, read by the 8051
5	SLP_EN	This bit is R/W by the Host; reads by the Host always return ‘0’. This bit can be set (written as ‘1’) but not cleared by the Host (writing ‘0’ has no effect). This bit is R/W by the 8051, and reads by the 8051 return the true value of the bit. When set by the Host, this bit is cleared by the 8051 writing a ‘1’ to it; writing ‘0’ has no effect.
6-7	RESERVED	RESERVED bits cannot be written and return “0” when read.

nEC_SCI INTERFACE

The nEC_SCI pin logic hardware is shown below in FIGURE 42.

Any or all of the PWRBTN_STS, SLPBTN_STS, and RTC_STS bits in the PM1_STS 2 register can assert the nEC_SCI pin if enabled by the PWRBTN_EN, SLPBTN_EN, and RTC_EN bits in the PM1_EN 2 register. See descriptions of these registers, above.

The 8051_SCI_STS bit can assert the nEC_SCI pin at any time, without being enabled. The 8051_SCI_STS bit is located in the 8051_PM_STS register at MMCR address 0x7F83h (TABLE 200).

The 8051_SCI_STS bit is in the FDC37N972 and is read/write by the 8051. If the 8051_SCI_STS bit is "1", an interrupt is generated on the nEC_SCI pin.

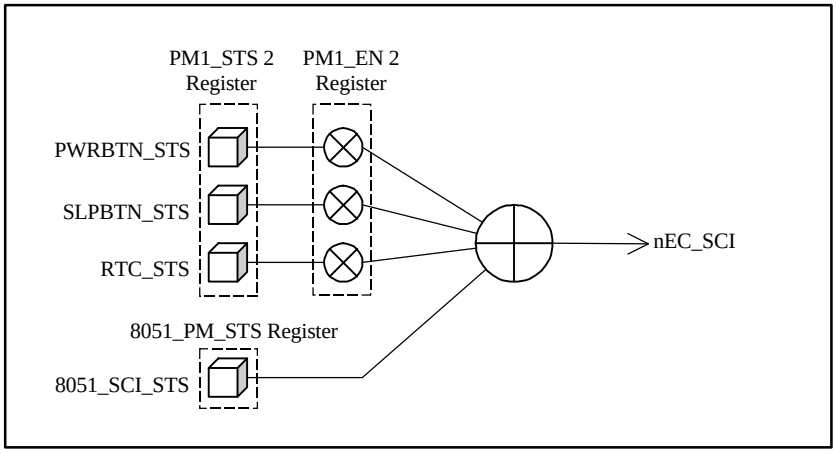


FIGURE 45 - HARDWARE nEC_SCI INTERFACE

TABLE 200 - 8051_PM_STS REGISTER

HOST ADDRESS	8051 ADDRESS	POWER PLANE	DEFAULT
-	0x7F83	VCC1	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
HOST TYPE	-	-	-	-	-	-	-	-
8051 TYPE	R	R	R	R	R	R	R	R/W
BIT NAME	RESERVED (RESERVED bits cannot be written and return "0" when read)							8051_ SCI_STS

REAL TIME CLOCK

GENERAL DESCRIPTION

The Real Time Clock Supercell (RTC) is a complete time of day clock with alarm, day of month alarm, one hundred year calendar, a century byte, and a programmable periodic interrupt. The RTC address space consists of two-128 bytes.banks of CMOS RAM (Bank0 and Bank1.) Each bank is accessable via address and data ports. These access ports have relocatable addresses and are acessable by both the host and the 8051. Each bank's last addressable location accesses the Shared RTC Control. The remaining 127 bytes of Bank0 contain the following: eleven registers of time, calendar, century, and alarm data, four control and status registers, and 111 bytes of general purpose registers. The remaining 127bytes of Bank1 contain general purpose registers.

FEATURES:

Allow 32kHz clock input or a 32kHz crystal.

Counts seconds, minutes, and hours of the day.

Counts days of the week, date, month and year.

Binary or BCD representation of time, calendar and alarm.

24 hour daily alarm.

30-day alarm.
RTC/CMOS Bank Addresses are relocatable.

The RTC CMOS Bank0 index register (70h) is shadowed

RTC Interrupt (IRQ8) is available on the parallel nIRQ8 pin.

RTC power source is switched internally between the VCC1 and VCC0 pins according to VCC1_PWRGD (See FIGURE 4 - VCC2 POWER-UP TIMING and FIGURE 5 – VCC1 PWRGD TIMING).

Lockable CMOS Ram Address Ranges (See Table 223 - RTC, LOGICAL DEVICE 6 [LOGICAL DEVICE NUMBER = 0X06]

CONFIGURATION REGISTERS

The RTC configuration registers, in Logical Device Number 6, provide activation control and the base address for the run-time registers (See TABLE 201)

The activate bit register 0x30, Bit D0 enables RTC/CMOS Bank0.

The activate bit register 0x30, Bit D1 enables RTC/CMOS Bank1.

TABLE 201 - RTC CONFIGURATION REGISTERS

INDEX	TYPE	HARD RESET	SOFT RESET	VCC2 POR	VCC1&VCC0 POR	DESCRIPTION							
						D7	D6	D5	D4	D3	D2	D1	D0
0x30	R/W	0x00	0x00	0x00	-	Activate							
						RESERVED						Activate CMOS Bank1	Activate RTC/ CMOS Bank0
0x60	R/W	0x00	0x00	0x00	-	RTC/CMOS Bank0 Primary Base Address High Byte							
						"0"	"0"	"0"	"0"	A11	A10	A9	A8
0x61	R/W	0x70	0x70	0x70	-	RTC/CMOS Bank0 Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	A2	A1	"0"
0x62	R/W	0x00	0x00	0x00	-	CMOS Bank1 Primary Base Address High Byte							
						"0"	"0"	"0"	"0"	A11	A10	A9	A8
0x63	R/W	0x74	0x74	0x74	-	CMOS Bank1 Primary Base Address Low Byte							
						A7	A6	A5	A4	A3	A2	A1	"0"
0xF1	R	-	-	-	-	Shadow RTC/CMOS Bank 0 Index register							

ISA HOST I/O INTERFACE

Each bank has a CMOS Address Register and a CMOS Data Register. Each bank's CMOS Address Register is located at the corresponding base address setup by the Configuration Registers in TABLE 201. Each bank's CMOS Data Register is located at an offest of the coresponding base (see TABLE 202.) Bit D7 of both CMOS Address Registers is not used for the CMOS RAM address decoding. All four CMOS Run Time regesters are fully read/write.

TABLE 202 - CMOS RUN TIME REGISTERS

ISA ADDRESS*	BANK	FUNCTION
Bank0 * (R/W)	RTC/CMOS Bank0	CMOS Address Register
Bank0 * + 1(R/W)	RTC/CMOS Bank0	CMOS Data Register
Bank1 * (R/W)	CMOS Bank1	CMOS Address Register
Bank1 * + 2(R/W)	CMOS Bank1	CMOS Data Register

INTERNAL REGISTERS

TABLE 203 shows the address map of the RTC and CMOS RAM, eleven registers of time, calendar, century , and alarm data, four control and status registers , 239 bytes of CMOS registers and one :Shared RTC Control register. Each bank's last addressable location accesses the same reigister: Shared RTC Control.

TABLE 203 - RTC AND CMOS RAM ADDRESS MAP

BANK	BASE OFFEST	REGISTER TYPE	REGISTER FUNCTION
Bank0	0	R/W	Register 0: Seconds
Bank0	1	R/W	Register 1: Seconds Alarm
Bank0	2	R/W	Register 2: Minutes
Bank0	3	R/W	Register 3: Minutes Alarm
Bank0	4	R/W	Register 4: Hours
Bank0	5	R/W	Register 5: Hours Alarm
Bank0	6	R/W	Register 6: Day of Week
Bank0	7	R/W	Register 7: Day of Month
Bank0	8	R/W	Register 8: Month
Bank0	9	R/W	Register 9: Year
Bank0	A	R/W	Register A:
Bank0	B	R/W	Register B: (Bit 0 is Read Only)
Bank0	C	R	Register C:
Bank0	D	R/W	Register D: Day of Month Alarm
Bank0	32	R/W	Century Byte
Bank0	E-31, 33-7F	R/W	General purpose
Bank0	7F	R/W	: Shared RTC Control
Bank1	0-7E	R/W	Bank 1: General purpose
Bank1	7F	R/W	: Shared RTC Control

All 256 bytes are directly writable and readable by the host with the following exceptions:

Registers C is read only
Bit 7 of Register D is read only which can only be set by a read of Register D.
Bit 6 of Register D is read only .
Bit 7 of Register A is read only
Bits 0 of Register B is read only
Bits 7-1 of the Shared RTC Control register are read only

TIME CALENDAR AND ALARM

The processor program obtains time and calendar information by reading the appropriate locations. The program may initialize the time, calendar and alarm by writing to these locations. The contents of the twelve time, calendar and alarm registers can be in binary or BCD as shown in **TABLE 204 - RTC REGISTER VALID RANGE**.

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the twelve locations in the binary or BCD format as defined by the DM bit in Register B. The SET bit may then be cleared to allow updates.

The 12/24 bit in Register B establishes whether the hour locations represent 1 to 12 or 0 to 23. The 12/24 bit cannot be changed without reinitializing the hour locations. When the 12 hour format is selected, the high order bit of the hours byte represents PM when it is a "1".

Once per second, the twelve time, calendar and alarm registers are updated, Incrementing by one second and checking for an alarm condition. During the update cycle all the registers in **TABLE 204**, except Register D, are not accessible by the processor program. The update cycle time is shown in Table **TABLE 205**. The update logic contains circuitry for automatic end-of-month recognition as well as automatic leap year compensation.

The three alarm registers may be used in two ways. First, when the program inserts an alarm time in the appropriate hours, minutes and seconds alarm locations, the alarm interrupt is initiated at the specified time each day if the alarm enable bit is high. The second usage is to insert a "don't care" state in one or more of three alarms registers. The "don't care" code is any hexadecimal byte from C0 to FF inclusive. That is the two most significant bits of each byte, when set to "1" create a "don't care" situation. An alarm interrupt each hour is created with a "don't care" code in the hours alarm location. Similarly, an alarm is generated every minute with "don't care" codes in the hours and minutes alarm bytes. The "don't care" codes in all three alarm bytes create an interrupt every second.

TABLE 204 - RTC REGISTER VALID RANGE

ADD	REGISTER FUNCTION	BCD RANGE	BINARY RANGE
0	Register 0: Seconds	00-59	00-3B
1	Register 1: Seconds Alarm	00-59	00-3B
2	Register 2: Minutes	00-59	00-3B
3	Register 3: Minutes Alarm	00-59	00-3B
4	Register 4: Hours	01-12 am	01-0C
	(12 hour mode)	81-92 pm	81-8C
	(24 hour mode)	00-23	00-17
5	Register 5: Hours Alarm	01-12 am	01-0C
	(12 hour mode)	81-92 pm	81-8C
	(24 hour mode)	00-23	00-17
6	Register 6: Day of Week	01-07	01-07
7	Register 7: Day of Month	01-31	01-1F

ADD	REGISTER FUNCTION	BCD RANGE	BINARY RANGE
8	Register 8: Month	01-12	01-0C
9	Register 9: Year	00-99	00-63
D	Day of Month Alarm	01-31	01-1F
32	Century Byte	00-99	00-63

UPDATE CYCLE

An update cycle is executed once per second if the SET bit in Register B is clear and the DV0-DV2 divider is not clear. The SET bit in the "1" state permits the program to initialize the time and calendar registers by stopping an existing update and preventing a new one from occurring.

The primary function of the update cycle is to increment the seconds register, check for overflow, increment the minutes register when appropriate and so forth through to the year of the century byte. The update cycle also compares each alarm register with the corresponding time register and issues an alarm if a match or if a "don't care" code is present.

The length of an update cycle is shown in **TABLE 205**. During the update cycle the time, calendar and alarm registers are not accessible by the processor program. If the processor reads these locations before the update cycle is complete the output will be undefined. The UIP (update in progress) status bit is set during the interval. When the UIP bit goes high, the update cycle will begin 244 µs later. Therefore, if a low is read on the UIP bit the user has at least 244 µs before time/calendar data will be changed.

TABLE 205 - RTC UPDATE CYCLE TIMING

INPUT CLOCK FREQUENCY	UIP BIT	UPDATE CYCLE TIME	MINIMUM TIME BEFORE START OF UPDATE CYCLE
32.768 kHz	1	1948 µs	-
32.768 KHZ	0	-	244 µs

CONTROL AND STATUS REGISTERS

The RTC has four registers, which are accessible to the processor program at all times, even during the update cycle.

REGISTER A

B7	B6	B5	B4	B3	B2	B1	B0
UIP	DV2	DV1	DV0	RS3	RS2	RS1	RS0

UIP

The update in progress bit is a status flag that may be monitored by the program. When UIP is a "1" the update cycle is in progress or will soon begin. When UIP is a "0" the update cycle is not in progress and will not be for at least 244 µs. The time, calendar, and alarm information is fully available to the program when the UIP bit is “0”. The UIP bit is a read only bit and is not affected by VCC1 POR. Writing the SET bit in Register B to a "1" inhibits any update cycle and then clears the UIP status bit.

DV2-0

Three bits are used to permit the program to select various conditions of the 22 stage divider chain. **TABLE 206** shows the allowable combinations. The divider selection bits are also used to reset the divider chain. When the time/calendar is first initialized, the program may start the divider chain at the precise time stored in the registers. When the divider reset is removed the first update begins one-half second later. These three read/write bits are not affected by VCC1 POR.

TABLE 206 - RTC DIVIDER SELECTION BITS

OSCILLATOR FREQUENCY	REGISTER A BITS			MODE
	DV2	DV1	DV0	
	0	0	0	Oscillator Disabled
32.768 kHz	0	0	1	Oscillator Disabled
32.768 kHz	0	1	0	Normal Operate
32.768 kHz	0	1	1	Test
32.768 kHz	1	0	X	Test
	1	1	X	Reset Divider

RS3-0

The four rate selection bits select one of 15 taps on the divider chain or disable the divider output. The selected tap determines rate or frequency of the periodic interrupt. The program may enable or disable the interrupt with the PIE bit in Register B. **Table 207** lists the periodic interrupt rates and equivalent output frequencies that may be chosen with the RS0-RS3 bits. These four bits are read/write bits which are not affected by VCC1 POR.

TABLE 207 - RTC PERIODIC INTERRUPT RATES

RATE SELECT	32.768 kHz TIME BASE	
RS3 RS2 RS1 RS0	PERIOD RATE OF INTERRUPT	FREQUENCY OF INTERRUPT
0 0 0 0	0.0	
0 0 0 1	3.90625 ms	256 Hz
0 0 1 0	7.8125 ms	128 Hz
0 0 1 1	122.070 µs	8.192 Hz
0 1 0 0	244.141 µs	4.096 kHz
0 1 0 1	488.281 µs	2.048 kHz
0 1 1 0	976.562 µs	1.024 kHz
0 1 1 1	1.953125 ms	512 Hz
1 0 0 0	3.90625 ms	256 Hz
1 0 0 1	7.8125 ms	128 Hz
1 0 1 0	15.625 ms	64 Hz
1 0 1 1	31.25 ms	32 Hz
1 1 0 0	62.5 ms	16 Hz
1 1 0 1	125 ms	8 Hz
1 1 1 0	250 ms	4 Hz
1 1 1 1	500 ms	2 Hz

REGISTER B

B7	B6	B5	B4	B3	B2	B1	B0
SET	PIE	AIE	UIE	RES	DM	24/12	DSE

SET

When the SET bit is a "0", the update functions normally by advancing the counts once-per-second. When the SET bit is a "1", an update cycle in progress is aborted and the program may initialize the time and calendar bytes without an update occurring in the middle of initialization. SET is a read/write bit, which is not modified by VCC1 POR or any internal functions.

PIE

The periodic interrupt enable bit is a read/write bit which allows the periodic-interrupt flag (PF) bit in Register C to cause the IRQB port to be driven low. The program writes a "1" to the PIE bit in order to receive periodic interrupts at the rate specified by the RS3 - RS0 bits in Register A. A “0” in PIE blocks IRQB from being initiated by a periodic interrupt, but the periodic flag (PF) is still set at the periodic rate. PIE is not modified by any internal function, but is cleared to "0" by a VCC1 POR.

AIE

The alarm interrupt enable bit is a read/write bit, which when set to a "1" permits the alarm flag (AF) bit in Register C to assert IRQB. An alarm interrupt occurs for each second that the three time bytes equal the three alarm bytes (including a "don't care" alarm code of binary 11XXXXXX). When the AIE bit is a "0", the AF bit does not initiate an IRQB signal. The VCC1 POR port clears AIE to "0". The AIE bit is not affected by any internal functions.

UIE

The update-ended interrupt enable bit is a read/write bit which enables the update-end flag (UF) bit in Register C to assert IRQB. The VCC1 POR port or the SET bit going high clears the UIE bit.

RES

Reserved - read as zero

DM

The data mode bit indicates whether time and calendar updates are to use binary or BCD

Formats: The DM bit is written by the processor program and may be read by the program, but is not modified by any internal functions or by VCC1 POR. A "1" in DM signifies binary data, while a "0" in DM specifies BCD data.

24/12

The 24/12 control bit establishes the format of the hours byte as either the 24 hour mode if set to a "1", or the 12 hour mode if cleared to a "0". This is a read/write bit that is not affected by VCC1 POR or any internal function.

DSE

The daylight savings enable bit is read only and is always set to a "0" to indicate that the daylight savings time option is not available.

REGISTER C

REGISTER C IS A READ ONLY REGISTER

B7	B6	B5	B4	B3	B2	B1	B0
IRQF	PF	AF	UF	0	0	0	0

IRQF

The interrupt request flag is set to a "1" when one or more of the following are true:
PF = PIE = 1
AF = AIE = 1
UF = UIE = 1

Any time the IRQF bit is a "1", the IRQB signal is driven low. All flag bits are cleared after Register C is read or by the VCC1 POR port.

PF

The periodic interrupt flag is a read only bit which is set to a "1" when a particular edge is detected on the selected tap of the divider chain. The RS3 -RS0 bits establish the periodic rate. PF is set to a "1" independent of the state of the PIE bit. PF being a "1" sets the IRQF bit and initiates an IRQB signal when PIE is also a "1". The PF bit is cleared by VCC1 POR or by a read of Register C.

AF

The alarm interrupt flag when set to a "1" indicates that the current time has matched the alarm time. A "1" in AF causes a "1"to appear in IRQF and the IRQB port to go low when the AIE bit is also a "1". A VCC1 POR or a read of Register C clears the AF bit.

UF

The update-ended interrupt flag bit is set after each update cycle. When the UIE bit is also a "1", the "1" in UF causes the IRQF bit to be set and asserts IRQB. A VCC1 POR or a read of Register C causes UF to be cleared.

B3-0

The unused bits of Register C are read as “0” and cannot be written.

REGISTER D

MSB LSB

b7	b6	b5	b4	b3	b2	b1	B0
VRT	0	Day of month					

VRT

The Valid RAM and Time (VRT) bit is cleared by the RTC to indicate that both the main power (VCC1) and the battery power (VCC0) are both low at the same time. This is the only case where the contents of the RAM,as well as, the time and calendar registers are not valid. The VRT bit can only be set by a read of Register D. The 8051 can set the VRT bit reading Register D after both of the following condition are met: VCC1_PWRGD =1 and the 8051 completes initialization. The Host can set the VRT bit reading Register D after PWRGD =1 See Section 0 Power Management.

B6

Read as zero and cannot be written.

B5:B0

Day of month Alarm; these bits store the day of month alarm value. If set to 000000b, then a don’t care state is assumed. The host must configure the Day of month alarm for these bits to do anything, yet they can be written at any time. If the Day of month alarm is not enabled, these bits will return zeros. These bits are not affected by RESET_DRV, VCC1_POR or VCC2_POR. The BCD Range for the Day of

month of month alarm is 1-31 and the Binary Range is 01-1F.

CENTURY BYTE

The century byte is located at RTC/Bank0 register 0x32. The century byte is incremented by one when the year byte changes from 99 or 0x63 to 0. The BCD Range for the century byte is 00-99 and the Binary Range is 00-63.

GENERAL PURPOSE

Registers 0xEh-0x7EH, except 0x32 (The Century Byte) in Bank0 and 0x0-0x7E in Bank1 are general purpose "CMOS" registers. These registers can be used by the host or 8051 and are fully available during the time update cycle. The contents of these registers are preserved by VCC0 power. Registers Eh-7Eh are in bank0 and registers 80h-FEh are in bank1.

SHARED RTC CONTROL

Each bank's last addressable location (0x7F) accesses the Shared RTC Control. The Shared RTC Control Register implements an interface that allows the 8051 to read/write the RTC and CMOS registers by use of the smart host protocol. Refer to 8051 RTC CMOS ACCESS Section for the definition of this register.

INTERRUPTS

The RTC includes three separate fully automatic sources of interrupts to the processor. The alarm interrupt may be programmed to occur at rates from one-per-second to one-a-day. The periodic interrupt may be selected for rates from half-a-second to 122.070 μs. The update ended interrupt may be used to indicate to the program that an update cycle is completed. Each of these independent interrupts are described in greater detail in other sections. The processor program selects which interrupts, if any, it wishes to receive by writing a "1" to the appropriate enable bits in Register B. A "0" in an enable bit prohibits the IRQB port from being asserted due to that interrupt cause. When an interrupt event occurs a flag bit is set to a "1" in Register C, which are set independent of the state of the corresponding enable bits in Register B. Each of the three interrupt sources have separate flag bits in Register C. The flag bits may be used with or without enabling the corresponding enable bits. The flag bits in Register C are cleared (record of the interrupt event is erased) when Register C is read. Double latching is included in Register C to ensure the bits that are set are stable throughout the read cycle. All bits which are high when read by the program are cleared, and new interrupts are held until after the read cycle. If an interrupt flag is already set when the interrupt becomes enabled, the IRQB port is immediately activated, though the interrupt initiating the event may have occurred much earlier.

When an interrupt flag bit is set and the corresponding interrupt-enable bit is also set, the IRQB port is driven low. IRQB is asserted as long as at least one of the three interrupt sources has its flag and enable bits both set. The IRQF bit in Register C is a "1" whenever the IRQB port is being driven low.

FREQUENCY DIVIDER

The RTC has 22 binary divider stages following the clock input. The output of the divider is a 1-Hertz signal to the update-cycle logic. The divider is controlled by the three divider bits (DV3-DV0) in Register A. As shown in Table 206 the divider control bits can select the operating mode, or be used to hold the divider chain reset that allows precision setting of the time. When the divider chain is changed from reset to the operating mode, the first update cycle is one-half second later.

PERIODIC INTERRUPT SELECTION

The periodic interrupt allows the IRQB port to be triggered from once every 500 ms to once every 122.07 µs. As Table 207 shows, the periodic interrupt is selected with the RS0-RS3 bits in Register A. The periodic interrupt is enabled with the PIE bit in Register B.

8051 RTC CMOS ACCESS

The FDC37N972FR implements an interface that allows the 8051 to read/write the RTC and CMOS registers under the following conditions: When nRESET_OUT is active, or when VCC2 is off, or by use of the smart host protocol.

RTCCNTRL (RTC CONTROL) REGISTER

Host	N/A
8051	0x7FF5
Power	VCC1
Default	0x80

The RTC Control register is mirrored in CMOS register 0x7Fh in both bank0 and bank1.

D7	D6	D5	D4	D3	D2	D1	D0
nSH	0	0	0	KREQH	HREQH	KREQL	HREQL

NSH

nSmart Host - This bit is controlled by the 8051. When set to a “1”, the host is not a smart host and does not recognize the sharing protocol. When set to a “0”, the host is smart and can recognize the sharing protocol. When set to “1”, this bit will clear HREQH and HREQL. Clearing this bit to “0” will allow the 8051 to regain access to the CMOS RAM.

KREQL

Keyboard Request Low - The 8051 can set this bit when HREQL IS '0'. If the request is not granted, this bit is read back as a zero and the request must be tried again. Note: After regaining control of the CMOS, the 8051 must re-write the RTC Low Address Register before accessing the RTC Data Register. This bit selects access to the CMOS RAM Addresses 0-7F.

HREQL

Host Request Low - This bit can be set by the host when KREQL is “0”. If the request is not granted, this bit is read back as a “0” and the request must be tried again.

KREQH

Keyboard Request High - This bit can be set by the 8051 when HREQH is “0” If the request is not granted, this bit is read back as a “0” and the request must be tried again. Note: After regaining control of the CMOS, the 8051 must re-write the RTC High Address Register before accessing the RTC Data Register. This bit selects access to the CMOS RAM Addresses 80-FF.

HREQH

Host Request High - This bit can be set by the host when KREQH is “0”. If the request is not granted, this bit is read back as a “0” and the request must be tried again.

nSH	KREQX	HREQX	BUS ACCESS
1	X	X	Host
0	0	0	None
0	1	0	8051
0	0	1	Host

RTC ADDRESS REGISTER (HIGH AND LOW)

Host	N/A
8051	0x7FF8 & 0x7FF6
Power	VCC1
Default	0x00 & 0x00

When KREQ=1.in the RTC Control register, the Low Address Register and the High Address Register are used to access the 256 CMOS RAM registers. The Low Address Register is used to provide the address to access the 128 CMOS RAM registers in bank0 and the High Address Register is used to provide the address to access the 128 CMOS RAM registers in bank1. Bit D7 of the Low Address Register and the High Address Register are not used for the address decode and are don’t care bits.

RTC DATA REGISTER (HIGH AND LOW)

Host	N/A
8051	0x7FF9 & 0x7FF7
Power	VCC1
Default	0x00 & 0x00

The low register is used to access the first bank of 128 bytes, in CMOS RAM the high register is used to access the second bank of 128 registers. This register is used to read or write the selected CMOS register when KREQ=1.

32kHz CLOCK INPUT

The FDC37N972 uses the XOSEL pin to select either a 32.768kHz input clock or a 32.768kHz crystal to drive the Real Time Clock Interface (TABLE 2 **- PIN FUNCTION DESCRIPTION**).

When XOSEL = '0', the RTC uses a 32.768kHz crystal connected between the XTAL1 and XTAL2 pins. When XOSEL = '1', the RTC is driven by a 32.768kHz single-ended clock source connected to the XTAL2 pin.

NOTE: $I_{CC0} \geq 10\mu A$ for time-keeping operations under V_{CC0} using a single-ended clock source. $I_{CC1} = 30\mu A$ under V_{CC1} using a single-ended clock source.

POWER MANAGEMENT

The RTC and CMOS RAM utilize VCC0 power plane (See **FIGURE 4 - VCC2 POWER-UP TIMING** and **FIGURE 5 - VCC1_PWRGD TIMING)**

The VCC1 POR does not affect the clock, calendar, or RAM functions. When VCC1 POR is active the following occurs:

Periodic Interrupt Enable (PIE) is cleared to "0".
Alarm Interrupt Enable (AIE) bit is cleared to "0".
Update Ended Interrupt Enable (UIE) bit is cleared to "0".
Update Ended Interrupt Flag (UF) bit is cleared to "0".
Interrupt Request status Flag (IRQF) bit is cleared to "0".
Periodic Interrupt Flag (PIF) is cleared to "0".
The RTC and CMOS registers are not accessible.
Alarm Interrupt Flag (AF) is cleared to "0".
nIRQ pin is in high impedance state.

If both the main power (VCC1) and the battery power (VCC0) are both low at the same time and then re-applied (ie. a new battery is installed) the following occurs:

Initialize all registers 00-0D to a "00" when VCC1 is applied.
The oscillator is disabled immediately.
The VRT bit is cleared to "0".

When PWRGD = 0, all host inputs are locked out so that the internal registers cannot be modified by the host system. The Host lockout condition continues for 500usec (min) to 1msec (max) after PWRGD =1. The Host lockout condition does not occur when either of the following occur:

RTC Divider Selection mode is not in normal mode in **TABLE 206**.
The VRT bit in Register D is a "0".

PCI CLOCK RUN SUPPORT

OVERVIEW

The FDC37N972 supports the PCI nCLKRUN signal. nCLKRUN is used to indicate the PCI clock status as well as to request that a stopped clock be started. See FIGURE 46 for an example of a typical system implementation using nCLKRUN.

nCLKRUN support is required because the FDC37N972 interrupt interface relies entirely on Serial IRQs. If an interrupt occurs while the PCI clock is stopped, nCLKRUN must be asserted before the interrupt can be serviced.

If the FDC37N972 Serial IRQs are disabled, nCLKRUN support is also disabled (see SERIRQ MODE BIT FUNCTION on page 303).

The nCLKRUN pin is an open drain output and an input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the nCLKRUN function. *Using nCLKRUN* If nCLKRUN is sampled "high", the PCI clock is stopped or

stopping. If nCLKRUN is sampled “low”, the PCI clock is starting or started (running).

If a device in the FDC37N972 asserts or de-asserts an interrupt and nCLKRUN is sampled “high”, the FDC37N972 can request the restoration of the clock by asserting the nCLKRUN signal asynchronously (**TABLE 208**). The FDC37N972 holds nCLKRUN low until it detects two rising edges of the clock. After the second clock edge, the FDC37N972 must disable the open drain driver (FIGURE 47). The FDC37N972 must not assert nCLKRUN if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in FIGURE 47. The FDC37N972 will not assert nCLKRUN under any conditions if the Serial IRQs are disabled.

The FDC37N972 must not assert nCLKRUN unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (FIGURE 47).

TABLE 208 - FDC37N972 nCLKRUN FUNCTION

SIRQ_EN	INTERNAL INTERRUPT REQUEST	nCLKRUN	ACTION
0	X	X	None
1	NO CHANGE	X	None
	CHANGE[1]	0	None
		1	Assert nCLKRUN

NOTE[1] “Change” means either-edge change on any or all parallel IRQs routed to the Serial IRQ block. The “change” detection logic must run asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., “continuous” or “quiet”.

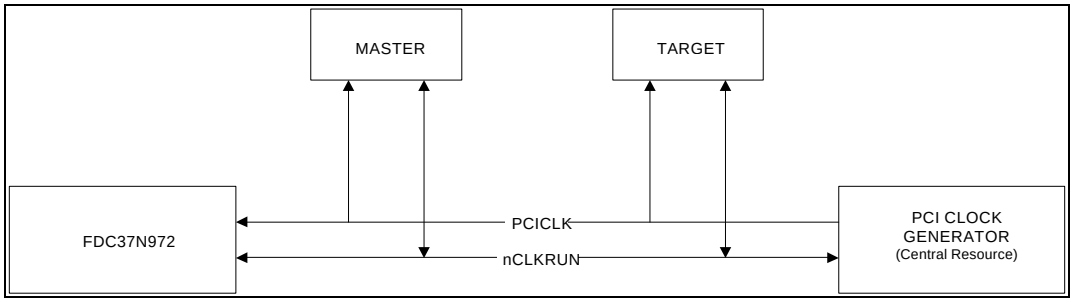


FIGURE 46 - nCLKRUN SYSTEM IMPLEMENTATION EXAMPLE

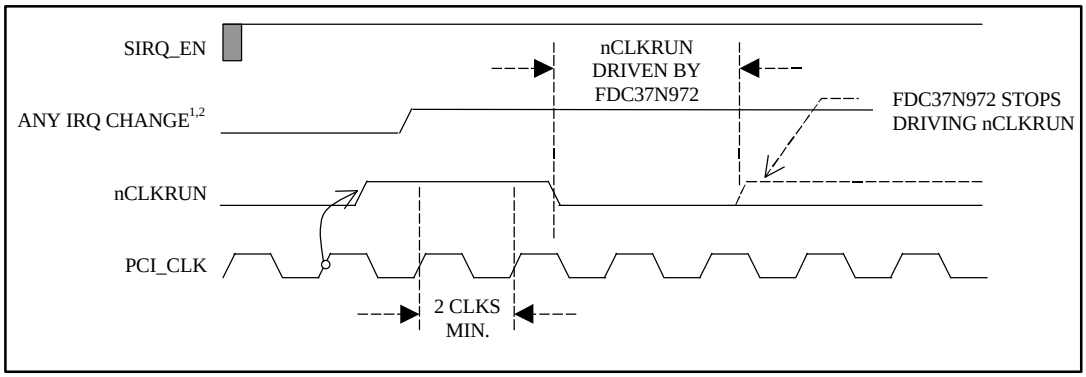


FIGURE 47 - CLOCK START ILLUSTRATION

NOTE[1] The signal “ANY IRQ CHANGE” is the same as “CHANGE” in **TABLE 208**.
NOTE[2] The FDC37N972 must continually monitor the state of nCLKRUN to maintain the PCI Clock until an active “ANY IRQ CHANGE” condition has been transferred to the host in a Serial IRQ cycle. For example, if “ANY IRQ CHANGE” is asserted before nCLKRUN is de-asserted (not shown in FIGURE 46), the FDC37N972 must assert nCLKRUN as needed until the Serial IRQ cycle has completed.

SERIAL INTERRUPTS

MSIO will support the serial interrupt scheme, which is adopted by several companies, to transmit interrupt information to the system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems Version 6.0.

Timing Diagrams For IRQSER Cycle

PCICLK = 33 MHz_IN pin
IRQSER = SIRQ pin

Start Frame timing with source sampled a low pulse on IRQ1.

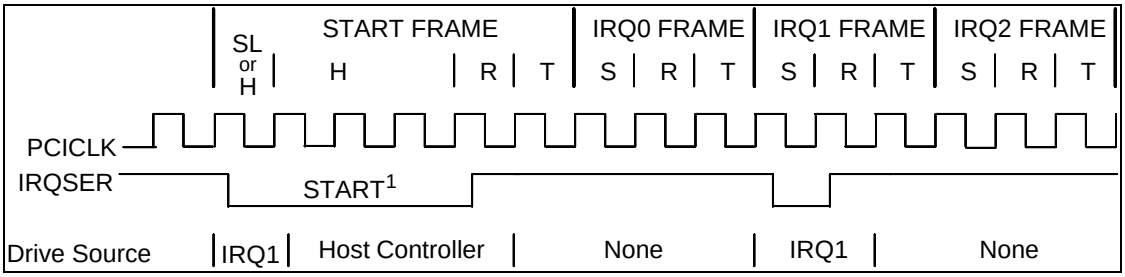


FIGURE 48 - SERIAL INTERRUPTS WAVEFORM "START FRAME"

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Start Frame pulse can be 4-8 clocks wide.

Stop Frame Timing with Host using 17 IRQSER sampling period

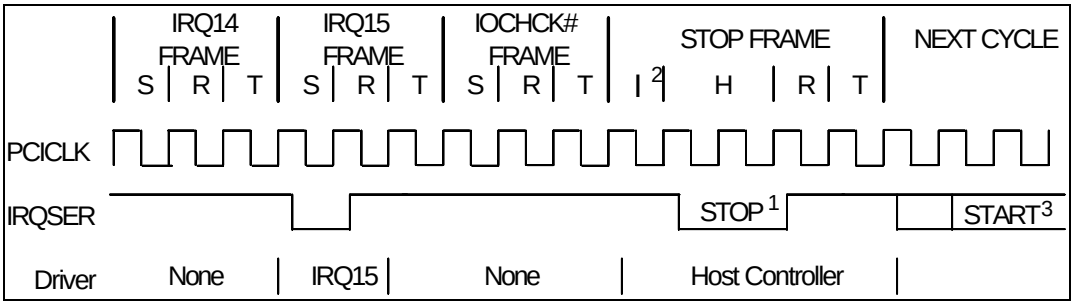


FIGURE 49 - SERIAL INTERRUPT WAVEFORM "STOP FRAME"

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle

Stop pulse is two clocks wide for Quiet mode, three clocks wide for Continuous mode.
There may be none, one or more Idle states during the Stop Frame.

The next IRQSER cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

SERIRQ MODE BIT FUNCTION

In the FDC37N972, the SERIRQ_EN (CR25.2) is used to enable the Serial IRQ interface (TABLE **209**). The SERIRQ_EN bit is also used to enable PCI Clock Run support (see Section PCI CLOCK RUN SUPPORTon page 300).

TABLE 209 - SERIRQ_EN CONFIGURATION CONTROL

CR25 BIT[2]	NAME	DESCRIPTION
0	SERIRQ_EN	Serial IRQ Disabled
1		Serial IRQ Enabled (Default)

IRQSER CYCLE CONTROL

There are two modes of operation for the IRQSER Start Frame.

QUIET (ACTIVE) MODE

Any device may initiate a Start Frame by driving the IRQSER low for one clock, while the IRQSER is Idle. After driving low for one clock the IRQSER must immediately be tri-stated without at any time driving high. A Start Frame may not be initiated while the IRQSER is active. The IRQSER is Idle between Stop and Start Frames. The IRQSER is active between Start and Stop Frames. This mode of operation allows the IRQSER to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the host controller will take over driving the IRQSER low in the next clock and will continue driving the IRQSER low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the host controller will drive the IRQSER back high for one clock then tri-state.

Any IRQSER Device (i.e., The FDC37N972) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the host controller unless the IRQSER is already in an IRQSER Cycle and the IRQ/Data transition can be delivered in that IRQSER Cycle.

CONTINUOUS (IDLE) MODE

Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other IRQSER agents become passive and may not initiate a Start Frame. IRQSER will be driven low for four to eight clocks by host controller. This mode has two functions. It can be used to stop or idle the IRQSER or the host controller can operate IRQSER in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An IRQSER mode transition can only occur during the Stop Frame. Upon reset, IRQSER bus is defaulted to continuous mode, therefore only the host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next IRQSER Cycle's mode.

IRQSER DATA FRAME

Once a Start Frame has been initiated, the FDC37N972 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the sample phase, the FDC37N972 must drive the IRQSER (SIRQ pin) low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, IRQSER must be left tri-stated. During the recovery phase the FDC37N972 must drive the SERIRQ high, if and only if, it had driven the IRQSER low during the previous sample phase. During the turn-around phase the FDC37N972 must tri-state the SERIRQ. The FDC37N972 drives the IRQSER line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the start frame.

The Sample phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, then the sample phase is {(6 x 3) - 1 = 17} the seventeenth clock after the rising edge of the Start Pulse.

TABLE 210 – IRQSER SAMPLING PERIODS

IRQSER PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	nSMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SIRQ data frame will now support IRQ2 from a logical device; previously IRQSER Period 3 was reserved for use by the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the FDC37N972 's SMI via the ESMI Mask Register. Likewise, when using Period 3 for nSMI, the user should not configure any logical devices as using IRQ2.

IRQSER Period 14 is used to transfer IRQ13. Logical devices 0 (FDC), 3 (Par Port), 4 (Ser Port 1), 5 (Ser Port 2), 6 (RTC), and 7 (KBD) will have IRQ13 as a choice for their primary interrupt.

STOP CYCLE CONTROL

Once all IRQ/Data Frames have completed the host controller will terminate IRQSER activity by initiating a Stop Frame. Only the host controller can initiate the Stop Frame. A Stop Frame is indicated when the IRQSER is low for two or three clocks. If the Stop Frame's low time is two clocks then the next IRQSER cycle's sampled mode is the Quiet mode; and any IRQSER device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks, then the next IRQSER cycle's sampled mode is the continuous mode, and only the host controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

LATENCY

Latency for IRQ/Data updates over the IRQSER bus in bridge-less systems with the minimum IRQ/Data Frames of seventeen will range up to 96 clocks (3.84µS with a 25 MHz PCI Bus or 2.88µs with a 33 MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR READ LATENCY

Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the IRQSER Cycle latency in order to ensure that these events do not occur out of order.

AC/DC SPECIFICATION ISSUE

All IRQSER agents must drive/sample IRQSER synchronously related to the rising edge of the PCI bus clock. IRQSER (SIRQ) pin uses the electrical specification of the PCI bus. Electrical parameters will follow the PCI specification section 4, sustained tri-state.

RESET AND INITIALIZATION

The IRQSER bus uses nPCIRST as its reset signal (nPCIRST is equivalent to using nRESET_OUT) and follows the PCI bus reset mechanism. The IRQSER pin is tri-stated by all agents while nPCIRST is active. With reset, IRQSER slaves and bridges are put into the (continuous) Idle mode. The host controller is responsible for starting the initial IRQSER cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent IRQSER cycles. It is the host controller's responsibility to provide the default values to the 8259's and other system logic before the first IRQSER cycle is performed. For IRQSER system suspend, insertion, or removal application, the host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee IRQSER bus is in Idle state before the system configuration changes.

XNOR-CHAIN TEST MODE

An XNOR-Chain test structure is in to the FDC37N972 to allow users to confirm that all pins are in contact with the motherboard during assembly and test operations (FIGURE 50).

The XNOR-Chain test structure must be activated to perform these tests. When the XNOR-Chain is activated, the FDC37N972 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR-Chain.

The tests that are performed when the XNOR-Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR-Chain output pin.

The XNOR-Chain test mode is activated and latched by:

nIOW = nIOR = nMEMWR = nMEMRD = "0"
AND
XOSEL = VCC1_PWRGD = PWRGD = "1"

The XNOR-Chain test mode is deactivated by VCC1_POR. All pins except for nRESET_OUT, XOSEL, XTAL1, XTAL2, and VCC1_PWRGD are included as inputs to the XNOR-Chain test structure. The XNOR-Chain output pin is nRESET_OUT.

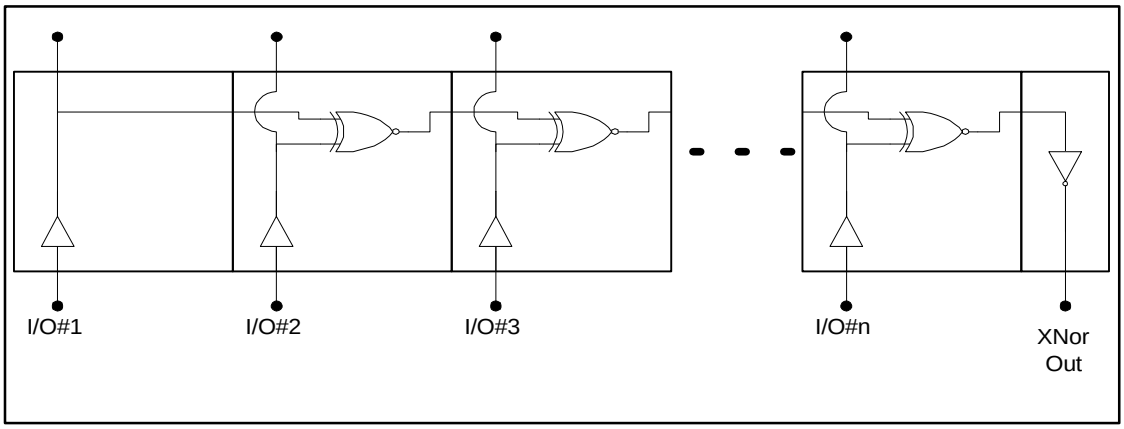


FIGURE 50 - XNOR-CHAIN TEST STRUCTURE

FDC37N972 CONFIGURATION

OVERVIEW

The Configuration of the FDC37N972 is very flexible and is based on the configuration architecture implemented in typical Plug-and-Play components.

The FDC37N972 is designed for motherboard designs in which the resources required by their components are known. With its flexible resource allocation architecture, the FDC37N972 allows the BIOS to assign resources at POST.

CONFIGURATION ELEMENTS

PRIMARY CONFIGURATION ADDRESS DECODER

The logical devices are configured through two Configuration I/O Ports (INDEX and DATA). The BIOS uses these Configuration Ports to initialize the logical devices at POST.

The MODE pin is a hardware configuration pin. The MODE pin sets the Configuration Port's default base address.
Note: All I/O addresses are qualified with AEN.

CONFIGURATION REGISTERS

CONFIGURATION REGISTER ACCESS

PRIMARY CONFIGURATION ADDRESS DECODER

The logical devices are configured through two Configuration Access Ports (INDEX and DATA). The BIOS uses these ports to initialize the logical devices at POST (TABLE 211).

The MODE pin is a hardware configuration pin that sets the default Configuration Access Port base address at power-up. The Configuration Ports base address can also be changed using the configuration ports base address register (see Configuration Registers BASE ADDRESS REGISTERS (VCC2) on page 308).

NOTE: All I/O addresses are qualified with AEN.

TABLE 211 - FDC37N972 CONFIGURATION ACCESS PORTS

PORT NAME	MODE PIN = 0 (10K PULL-DOWN RESISTOR OR TIE TO GND)	MODE PIN = 1 (10K PULL-UP RESISTOR OR TIE TO VCC1)	TYPE
CONFIG PORT	0x03F0 (Note 1)	0x0370 (Note 1)	Write (NOWS ISA I/O)
INDEX PORT	0x03F0 (Note 1)	0x0370 (Note 1)	Read/Write (NOWS ISA I/O)
DATA PORT	INDEX PORT + 1 (Note 1)		Read/Write (NOWS ISA I/O)

The INDEX and DATA ports are effective only when the chip is in the Configuration State.
Note 1: This address can be changed by configuration registers 26h and 27h.

Entering the Configuration State
The device enters the Configuration State when the following Config Key is successfully written to the CONFIG PORT.

Config Key = < 0x55>

Exiting the Configuration State

The device exits the Configuration State when the following Config Key is successfully written to the CONFIG PORT address.

Config Key = < 0xAA>

READ ACCESING CONFIGURATON PORT

The Configuration Port reads back a float condition when not in the Configuration State. The Configuration Port reads back 0x00, after the Configuration Key 0x55 has been written to the Configuration Port, but prior any further writes to the Configuration Port. After the Configuration Index Register has been written to at least once (in the Configuration State,) then the last value written to the Configuration Index Register (via the Configuration Port) can be read back.

CONFIGURATION REGISTERS BASE ADDRESS REGISTERS (VCC2)

The FDC37N972 configuration ports base address is relocatable beyond the two addressing options provided by the MODE pin.

Registers CR26 and CR27 enable the relocatable configuration ports base address function. CR26 is the configuration ports base address least significant byte; CR27 is the most significant byte (TABLE 212).

The configuration ports base address is relocatable on even-byte boundaries; i.e., A0 = "0". Valid configuration ports base address values are 0x0000 – 0x0FFE.

At power-up, the configuration ports base address is determined by the MODE pin. To relocate the configuration ports base address after power-up, first write the lower address byte (LSB) of the new base address to CR26 and then write the upper address bits to CR27. **NOTE:** writing CR27 changes the configuration ports base address.

The ability to relocate the configuration ports base address can prevent address conflicts, particularly when tape drives are used.

TABLE 212 - CONFIGURATION PORT ADDRESS REGISTERS

INDEX	TYPE	HARD RESET & VCC2 POR[1]	SOFT RESET, VCC1 POR & VCC0 POR	REGISTER NAME	DESCRIPTION							
					D7	D6	D5	D4	D3	D2	D1	D0
GLOBAL CONFIGURATION REGISTERS												
0x26[2]	R/W	MODE = 0: 0xF0 MODE = 1: 0x70	-	Configuration Port Base Address Byte 0 (LSB)	A7	A6	A5	A4	A3	A2	A1	"0"
0x27[3]	R/W	MODE = 0: 0x03 MODE = 1: 0x03	-	Configuration Port Base Address Byte 1 (MSB)	"0"	"0"	"0"	"0"	A11	A10	A9	A8

NOTE[1] The MODE pin determines the configuration port base address following Hard Reset and VCC2 POR.

NOTE[2] The configuration ports base address is relocatable on even-byte boundaries; i.e., A0 = "0".

NOTE[3] Writing CR27 changes the configuration ports base address.

The FDC37N972 Configuration register map is shown below in **TABLE 213**.

CONFIGURATION REGISTER RESET CONDITIONS

HARD RESET = VCC2 POR or RESET_OUT pin asserted.

SOFT RESET = Configuration Control Register Bit0 set to a one by host.

TABLE 213 - FDC37N972 CONFIGURATION REGISTER MAP

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER NAME
GLOBAL CONFIGURATION REGISTERS				
0x02	W	0x00	0x00	Config Control
0x03	-	-	-	RESERVED
0x07	R/W	0x00	0x00	Logical Device Number
0x17	-	-	-	RESERVED
0x20	R	0x0A	0x0A	FDC37N971
		0x0B	0x0B	FDC37N972
0x21	R	0x00	0x00	Device Rev - hard wired
0x22	R/W	0x00	n/a	Power Control
0x23	R/W	0x00	n/a	Power Mgmt
0x24	R/W	0x04	n/a	OSC
0x25	R/W	0x04	n/a	DeviceMode
0x26	R/W	See above		Configuration Port Base Address (LSB)
0x27	R/W	See above		Configuration Port Base Address (MSB)
0x28 – 0x2F	-	0x00	0x00	RESERVED (Test Mode Registers)
LOGICAL DEVICE 0 CONFIGURATION REGISTERS (FDC)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x03, 0xF0	0x03, 0xF0	Primary Base I/O Address
0x70	R/W	0x06	0x06	Primary Interrupt Select
0x74	R/W	0x02	0x02	DMA channel Select
0xF0	R/W	0x0E	n/a	FDD Mode Register
0xF1	R/W	0x00	n/a	FDD Option Register
0xF2	R/W	0xFF	n/a	FDD Type Register
0xF4	R/W	0x00	n/a	FDD0
0xF5	R/W	0x00	n/a	FDD1
LOGICAL DEVICE 1 CONFIGURATION REGISTERS (PM1)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
LOGICAL DEVICE 2 CONFIGURATION REGISTERS (RESERVED)				
LOGICAL DEVICE 3 CONFIGURATION REGISTERS (PARALLEL PORT)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	DMA channel Select
0xF0	R/W	0x3C	n/a	Parallel Port Mode Register
0xF1	R/W	0x00	n/a	Parallel Port CnfgB shadow Register

INDEX	TYPE	HARD RESET	SOFT RESET	CONFIGURATION REGISTER NAME
LOGICAL DEVICE 4 CONFIGURATION REGISTERS (SERIAL PORT 1)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	UART Register Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Serial Port 1 Mode Register
LOGICAL DEVICE 5 CONFIGURATION REGISTERS (INFRARED)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Primary Base I/O Address
0x62, 0x63	R/W	0x00, 0x00	0x00, 0x00	SCE Register Base I/O Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0x74	R/W	0x04	0x04	IRCC 2.0 DMA Channel Select
0xF0	R/W	0x00	n/a	Mode Register
0xF1	R/W	0x02	n/a	IR Options Register
0xF2	R/W	0x03	n/a	IR Half Duplex Timeout
0xF7	R/W	0x00	0x00	Software Select A
0xF8	R/W	0x00	0x00	Software Select B
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (RTC)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x70	0x00, 0x70	RTC Bank 0 Primary Base Address
0x62, 0x63	R/W	0x00, 0x74	0x00, 0x74	RTC Bank 1 Primary Base Address
0x70	R/W	0x00	0x00	Primary Interrupt Select
0xF0	R/W	0x00	n/a	Real Time Clock Mode Register
00xF1	R	-	-	Shadowed RTC/CMOS Bank 0 Index Register
LOGICAL DEVICE 7 CONFIGURATION REGISTERS (KBD)				
0x30	R/W	0x00	0x00	Activate
0x70	R/W	0x00	0x00	Primary Interrupt Select
0x72	R/W	0x00	0x00	Second Interrupt Select
0xF0	R/W	0x00	0x00	KRST_GA20
LOGICAL DEVICE 8 CONFIGURATION REGISTERS (EC)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x62	0x00, 0x62	ECI Register Base I/O Address
LOGICAL DEVICE 9 CONFIGURATION REGISTERS (MAILBOX)				
0x30	R/W	0x00	0x00	Activate
0x60, 0x61	R/W	0x00, 0x00	0x00, 0x00	Mailbox Register Base I/O Address

CHIP LEVEL (GLOBAL) CONTROL/CONFIGURATION REGISTERS [0X00-0X2F]

The chip-level (global) registers lie in the address range [0x00-0x2F].

The INDEX PORT is used to select a configuration register in the chip. The DATA PORT is then used to access the selected register. These registers are accessible only in the Configuration State.

TABLE 214 - GLOBAL CONFIGURATION REGISTERS

REGISTER	ADDRESS	DESCRIPTION	STATE
Chip (Global) Control Registers			
	0x00 - 0x01	Reserved, Writes are ignored, reads return 0.	
Config Control	0x02 W	The hardware automatically clears this bit after the write; there is no need for software to clear the bits. Bit [0] = 1: Soft Reset; Refer to TABLE 213 for the soft reset value for each register.	C
Card Level Reserved	0x03W	Reserved - Writes are ignored, reads return 0.	
	0x04 - 0x06	Reserved - Writes are ignored, reads return 0.	
Logical Device #	0x07 R/W	A write to this register selects the current logical device. This allows access to the control and configuration registers for each logical device. Note: The Activate command operates only on the selected logical device.	C
Card Level Reserved	0x08 - 0x1F	Reserved - Writes are ignored, reads return 0.	
Chip-Level, SMSC Defined			
Device ID Hard Wired	0x20 R	A read-only register which provides device identification. Bit[7-0] FDC37N971 = 0x0A FDC37N972 = 0x0B	C
Device Rev Hard Wired	0x21 R	A read-only register which provides device revision information. Bits[7-0] = 0x00 when read	C

REGISTER	ADDRESS	DESCRIPTION	STATE
PowerControl	0x22 R/W	Bit[0] FDC Power Bit[1:2] Reserved (read as 0) Bit[3] Parallel Port Power Bit[4] Serial Port 1 Power Bit[5] Serial Port 2 Power Bit[6:7] Reserved (read as 0) =0 Power off or disabled =1 Power on or Enabled	C
Power Mgmt	0x23 R/W	Bit[0] FDC Bit[1:2] Reserved (read as 0) Bit[3] Parallel Port Bit[4] Serial Port 1 Bit[5] Serial Port 2 Bit[6:7] Reserved (read as 0) =0 Power off or disabled =1 Power on or Enabled	C
OSC	0x24 R/W	Bit[1:0] Reserved, set to “0” Bit[3:2] OSC =01 OSC is on, BRG clock is on when PWRGD is active, OSC is off and BRG Clock is disabled (default) =10 Same as above (01) case =00 OSC is on, BRG Clock Enabled =11 OSC is off, BRG Clock is disabled Bit[6:4] CLK_OUT Select =[0,0,0] CLK_OUT = 1.8432 MHz =[0,0,1] CLK_OUT = 14.318 MHz =[0,1,0] CLK_OUT = 16 MHz =[0,1,1] CLK_OUT = 24 MHz =[1,0,0] CLK_OUT = 48 MHz =[1,0,1] Reserved =[1,1,X] Reserved Bit[7] nIRQ8 Polarity =0 nIRQ8 is active high =1 nIRQ8 is active low Note: This polarity bit not only affects the nIRQ8 pin, but is also reflected in the Serial IRQ sample phase for the IRQ8 Frame for the Serial IRQ Bus.	C

REGISTER	ADDRESS	DESCRIPTION	STATE
Device Mode	0x25 R/W	Bit [1-0] Flash Timing This register is used to program the width of Flash Read (nFRD) and Flash Write (nFWR) signals during Host Flash accesses. = 0,0 : nFRD/nFWR width = 3 sclks = 0,1 : width = 2.5 sclks = 1,0 : width = 2 sclks = 1,1 : Reserved, do not use. Bit[2] SerIRQ Mode = 0 : Serial IRQ Disabled. = 1 : Serial IRQ Enabled (Default). Bit [4:3] Parallel Port FDC = [0:0] Normal = [0:1] PPFD1 Mode = [1:0] PPFD2 Mode = [1:1] Reserved Bit [7:5] Reserved - writes ignored, reads return “0”.	
Chip Level Vendor Defined	0x26	Reserved - Writes are ignored, reads return 0.	
Test Registers	0x27-0x2B	SMSC Test Mode Registers, Reserved for SMSC.	
TEST 0	0x2C	Test Modes - Reserved for SMSC. Users should not write to this register, may produce undesired results.	
TEST 1	0x2D R/W	Test Modes : Reserved for SMSC. Users should not write to this register; may produce undesired results.	C
TEST 2	0x2E R/W	Test Modes - Reserved for SMSC. Users should not write to this register; may produce undesired results.	C
TEST 3	0x2F R/W	Test Modes - Reserved for SMSC. Users should not write to this register; may produce undesired results.	C

LOGICAL DEVICE CONFIGURATION/CONTROL REGISTERS [0X30-0XFF]

Used to access the registers that are assigned to each logical unit. This chip supports six logical units and has six sets of logical device registers. The logical devices are Floppy, Parallel, Serial 1 and IRCC 2.0

(UART), Real Time Clock, and Keyboard Controller. A separate set (bank) of control and configuration registers exists for each Logical Device and is selected with the Logical Device # Register (0x07).
The INDEX PORT is used to select a specific logical device register. These registers are then accessed through the DATA PORT.

The Logical Device registers are accessible only when the device is in the Configuration State The logical register addresses are listed in TABLE 215.

TABLE 215 - LOGICAL DEVICE CONFIGURATION REGISTERS

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Activate (1)	(0x30)	Bits[7:1] Reserved, set to “0”. Bit[0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive.	C
Bank Activation FOR RTC ONLY	(0x30) FOR RTC ONLY	Bits[7:2] Reserved, set to “0”. Bit[1] Activates Bank 1 Bit[0] Activates Bank 0 Bit[1:0] = 1 Activates the logical device currently selected through the Logical Device # register. = 0 Logical device currently selected is inactive.	
Logical Device Control	(0x31-0x37)	Reserved - Writes are ignored, reads return “0”.	C
Logical Device Control	(0x38-0x3f)	Vendor Defined – Reserved - Writes are ignored, reads return “0”.	C
Memory Base Address	(0x40-0x5F)	Reserved - Writes are ignored, reads return “0”.	C
I/O Base Address **(see Table 216)**	(0x60-0x6F) 0x60 = addr[15:8] 0x61= addr[7:0]	All logical devices contain 0x60, 0x61. Unused registers will ignore writes and return “0” when read.	C

LOGICAL DEVICE REGISTER	ADDRESS	DESCRIPTION	STATE
Interrupt Select	(0x70,072)	0x70 is implemented for each logical device. Refer to Interrupt Configuration Register description. Only the KYBD controller uses Interrupt Select register 0x72. Unused register (0x72) will ignore writes and return “0” when read. Interrupts default to edge high (ISA compatible).	C
	(0x71,0x73)	Reserved - not implemented. These register locations ignore writes and return “0” when read.	
DMA Channel Select	(0x74)	Only 0x74 is implemented for FDC , and Parallel port. Refer TABLE 218 - DMA CHANNEL SELECT CONFIGURATION REGISTERS.	C
	(0x75)	Reserved - not implemented and ignores writes and returns “0” when read.	
32-Bit Memory Space Configuration	(0x76-0xA8)	Reserved - not implemented. These register locations ignore writes and return “0” when read.	
Logical Device	(0xA9-0xDF)	Reserved - not implemented. These register locations ignore writes and return “0” when read.	C
Logical Device Configuration	(0xE0-0xFE)	Reserved - Vendor Defined (see SMSC defined Logical Device Configuration Registers).	C
Reserved	0xFF	Reserved	C

Note1: A logical device will be active and powered up according to the following equation:DEVICE ON (ACTIVE) = (Activate Bit SET AND Pwr/Control Bit SET) AND (8051 Disable Bit SET)

The Logical device's Activate Bit and its Pwr/Control Bit are linked such that setting or clearing one sets or clears the other. Three bits in the 8051’s Disable Register (see Keyboard spec), bits D7, D6 and D4 are capable of overriding the Activate and PWR/Control bit settings for logical devices 3, 4 and 0 respectivelely. Thus clearing bit D7 of the Disable register will disable the FDC regardless of the FDC’s Activate and PWR/Control bits. When D7 of the Disable register is set, the FDC’s Activate and PWR/Control bits will determine the on/off state of the FDC. If the I/O Base Addr of the logical device is not within the Base I/O range as shown in the Logical Device I/O map, then read or write is not valid and is ignored.

I/O BASE ADDRESS CONFIGURATION REGISTER DESCRIPTION

TABLE 216 - LOGICAL DEVICE, BASE I/O ADDRESSES

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
0x00	FDC	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : SRA +1 : SRB +2 : DOR +3 : TSR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
0x01	Reserved			
0x02	Reserved			
0x03	Parallel Port	0x60,0x61	[0x100:0x0FFC] ON 4 BYTE BOUNDARIES (EPP Not supported) or [0x100:0x0FF8] ON 8 BYTE BOUNDARIES (all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+0 : Data | ecpAfifo +1 : Status +2 : Control +3 : EPP Address * +4 : EPP Data 0 * +5 : EPP Data 1 * +6 : EPP Data 2 * +7 : EPP Data 3 * +400h : cfifo | ecpDfifo | tfifo | cnfgA +401h : cnfgB +402h : ecr
0x04	Serial Port 1	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB | LSB div +1 : IER | MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
0x05	IRCC 2.0 (UART)	0x60,0x61	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : RB/TB | LSB div +1 : IER | MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR

LOGICAL DEVICE NUMBER	LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (NOTE 1)	FIXED BASE OFFSETS
0x05	IRCC 2.0 (IR-SCE)	0x62, 0x63	[0x100:0x0FF8] ON 8 BYTE BOUNDARIES	+0 : Register Block N, address 0 +1 : Register Block N, address 1 +2 : Register Block N, address 2 +3 : Register Block N, address 3 +4 : Register Block N, address 4 +5 : Register Block N, address 5 +6 : Register Block N, address 6 +7: SCE Master Control Reg.
0x06	RTC	0x60, 0x61 0x62, 0x63	[0x00:0x0FFE] [0x00:0x0FFD]	Bank 0 Base address +0 : Address Register +1 : Data Register * Bank 1 Base address +0 : Address Register +2 : Data Register *
0x07	KYBD	N/a	Not Relocatable Fixed Base Address	0x60 : Data Register 0x64 : Command/Status Reg.
0x08	ECI	0x60, 0x61[2]	[0x0000:0xFFA] Relocatable	+0 : Data Register[3] +4 : COMMAND REGISTER
0x09	Mailbox Register	0x60, 0x61	[0x0000:0x0FFE]	+0 : Index +1 : Data

Note 1: This chip uses all ISA address bits to decode the base address of each of its logical devices.
Note 2: Please refer to **TABLE 49** for further description.
Note 3: Please refer to **TABLE 50** for further description.
Note*: When these registers are accessed the nNOWS line is not asserted. All other registers in this table assert the nNOWS signal when accessed.

INTERRUPT SELECT CONFIGURATION REGISTER DESCRIPTION

TABLE 217 - INTERRUPT SELECT CONFIGURATION REGISTERS

Name	Reg Index	Definition	State
Interrupt request level select 0	0x70 (R/W)	Bit [3-0] Select which interrupt level is used for Interrupt 0. 0x00=no interrupt selected. 0x01=IRQ1 0x02=IRQ2 • • • 0x0E= IRQ14 0x0F= IRQ15 All pin-type interrupts are edge high (except ECP/EPP). Each Logical Device's interrupts selected through this register physically select the interrupts to be used by the FDC37N972 for either the Serial IRQ interface or for the individual pin-type ISA interrupts if selected. Setting the IRQ through this register for the Parallel Port is not reflected in the Enhanced Parallel port cnfgB register, software must set the DMA/IRQ bits in the Parallel Port logical device config register 0xF1 (Parallel Port CnfgB shadow register).	C

Note : An interrupt is activated by setting the Interrupt Request Level Select 0 register to a non-zero value AND :

1. For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register.
2. For the PP logical device by setting IRQE, bit D4 of the Control Port and in addition
3. For the PP logical device in ECP mode by clearing serviceintr, bit D2 of the ecr.
4. For the Serial Port logical device by setting any combination of bits D0-D3 in the IER and by setting the OUT2 bit in the UART's Modem Control (MCR) Register.
5. For the RTC by (refer to the RTC section of this specification).
6. For the KYBD by (refer to the KYBD controller section of this specification).

DMA CHANNEL SELECT CONFIGURATION REGISTER DESCRIPTION

TABLE 218 - DMA CHANNEL SELECT CONFIGURATION REGISTERS

NAME	REG INDEX	DEFINITION	STATE
DMA Channel select 0	0x74 (R/W)	Bit [2:0] Select the DMA Channel. 0x00=DMA0 0x01=DMA1 0x02=DMA2 0x03=DMA3 0x04-0x07= No DMA active	C

Note: A DMA channel is activated by setting the DMA Channel Select 0 register to [0x00-0x03] AND :

1. For the FDC logical device by setting DMAEN, bit D3 of the Digital Output Register
2. For the PP logical device in ECP mode by setting dmaen, bit D3 of the ecr
3. For the UART2 logical device, by setting the DMA Enable bit. Refer to the IRCC 2.0 specification available from SMSC

Note: DMAREQ pins must tri-state if not used/selected by any Logical Device.

IRQ AND DMA ENABLE AND DISABLE

Any time the IRQ and/or DMA channels for a logical device are disabled by a register in that logical device, the IRQ and/or nDACK must be disabled. This is in addition to the IRQ and nDACK disabled by the Configuration Registers (activate bit cleared or address outside of valid range or the Interrupt Select register set to 0x00 or the DMA Channel Select register set to 0x04).

LOGICAL DEVICE 0 (FDC)

For the following cases, the IRQ and DACK used by the FDC are disabled (high impedance), i.e., will not respond to the DREQ Digital Output Register (Base+2) bit D3 (DMAEN) set to "0". The FDC is in power down (disabled).

LOGICAL DEVICE 5 (SERIAL PORT1)

Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", then the serial port interrupt is forced to a high impedance state - disabled.

LOGICAL DEVICE 5 (SERIAL PORT2/USART)

Interrupt is disabled when:

Modem Control Register (MCR) bit 2 (OUT2) - When OUT2 is a logic “0”, then Logical Device 5’s interrupt is forced to a high impedance state, i.e., disabled. This applies to all UART/IR modes of operation.

DRQ is disabled when:

SCE Configuration Register B bit-0 (DMA Enable) - When the DMA Enable bit is a logic “0”, then logical device 5’s DRQ pin is forced to a high impedance state, i.e., disabled. When the DMA Enable bit is set to logic “1”, then logical device 5’s DRQ pin is active and drives low until the device issues a DMA Request at which point the DRQ pin drives high. This eliminates the need for an external pull-down resistor on the logical device 5’s DRQ pin.

PARALLEL PORT

SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled (high impedance).

ECP Mode:
(DMA) dmaEn from ecr register.

IRQ - See table below.

MODE (FROM ECR REGISTER)		IRQ PIN CONTROLLED BY	PDREQ PIN CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn
111	CONFIG	IRQE	dmaEn

REAL TIME CLOCK (RTC)

(refer to the RTC section)

KEYBOARD CONTROLLER (KYBD)

(REFER TO THE KEYBOARD CONTROLLER SECTION)

SMSC DEFINED LOGICAL DEVICE CONFIGURATION REGISTERS

The SMSC Specific Logical Device Configuration Registers reset to their default values only on hard resets generated by VCC2 POR or the nRESET_OUT signal. These registers are not effected by soft resets.

TABLE 219 - FDC, LOGICAL DEVICE 0 [LOGICAL DEVICE NUMBER = 0X00]

NAME	REG INDEX	DEFINITION	STATE
FDD Mode Register Default = 0x0E	0xF0 R/W	Bit[0] Floppy Mode =0 Normal Floppy Mode (default) =1 Enhanced Floppy Mode 2 (OS2) Bit[1] FDC DMA Mode =0 Burst Mode is enabled =1 Non-Burst Mode (default) Bit[3:2] Interface Mode Bit 3 – IDENT Bit 2 – MFM =11 AT Mode (default) =10 (Reserved) =01 PS/2 =00 Model 30 Bit[4] Swap Drives 0,1 Mode =0 No swap (default) =1 Drive and Motor Sel 0 and 1 are swapped Bit[5] FDC Shutdown =0 FDC37N972 FDC operates normally, FDC pins are active (default) =1 FDC core is shutdown, only I/O Writes to DOR, TDR, DSR and CCR are enabled, all Floppy Disk interface pins tri-state except for DRVDEN0, DRVDEN1, nDS0, nDS1, nMTR0, and nMTR1. Bit[6] FDC Output Type Control =0 FDC Outputs are OD24 Open Drain (default) =1 FDC Outputs are O24 push pull Bit[7] FDC Output Control =0 FDC Outputs active (default) =1 FDC Outputs tri-stated Bits 6 and 7 do not reflect the Parallel Port FDC pins.	C
FDD Option Register Default = 0x00	0xF1 R/W	Bit[1:0] Reserved, set to “0” Bit[3-2] Density Select =00 Normal (default) =01 Normal (reserved for users) =10 (forced to logic “1”) =11 (forced to logic “0”) Bit[5:4] Reserved Bit[7:6] Boot Floppy =00 FDD 0 (default) =01 FDD 1 =10 FDD 2 =11 FDD 3	C

NAME	REG INDEX	DEFINITION	STATE
FDD Type Register Default = 0Xff	0xF2 R/W	Bit[1:0] Floppy Drive A Type Bit[3:2] Floppy Drive B Type Bit[5:4] Floppy Drive C Type Bit[7:6] Floppy Drive D Type	C
	0xF3 R	Reserved, read as 0 (read only)	C
FDD0 Default = 0x00	0xF4 R/W	Bit[1:0] Drive Type Select Bit[2] Read as “0” (read only) Bit[3:4] Data Rate Table Select Bit[5] Read as “0” (read only) Bit[6] Precomp Disable Bit[7] Read as “0” (read only)	C
FDD1	0xF5 R/W	Refer to definition and default for 0xF4	C

DT0	DT1	DRVDEN0 (1)	DRVDEN1 (1)	DRIVE TYPE
0	0	DENSEL	DRATE0	4/2/1 MB 3.5” 2/1 MB 5.25” FDDS 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	nDENSEL	DRATE0	
1	1	DRATE0	DRATE1	

There are four of the following registers in the configuration data space, one for each drive.
FDD0 - 0xF4/FDD1 - 0xF5

D7	D6	D5	D4	D3	D2	D1	D0
0	PTS	0	DRT1	DRT0	0	DT0	DT1

PTS = 0 Use Precompensation, = 1 No Precompensation

DTx = Drive Type Select
DRTx = Data Rate Table Select
DENSEL, DRATE1 and DRATE0 map onto three output pins DRVDEN0 and DRVDEN1.

TABLE 220 - PARALLEL PORT, LOGICAL DEVICE 3 [LOGICAL DEVICE NUMBER = 0X03]

NAME	REG INDEX	DEFINITION	STATE
PP Mode Register Default = 0x3C	0xF0 R/W	Bit [2:0] Parallel Port Mode = 100 Printer Mode (default) = 000 Standard and Bi-directional (SPP) Mode = 001 EPP-1.9 and SPP Mode = 101 EPP-1.7 and SPP Mode = 010 ECP Mode = 011 ECP and EPP-1.9 Mode = 111 ECP and EPP-1.7 Mode Bit[6:3] ECP FIFO Threshold 0111b (default) Bit[7] PP Interrupt Type Not valid when the parallel port is in the Printer Mode (100) or the Standard $ Bi-Directional Mode (000) =1 Pulsed Low, released to high-Z (665/666) =0 IRW follows nACK when parallel port in EPP Mode or [Printer, SPP, EPP] under ECP, TEST or Centronics FIFO Mode.	C
Parallel Port CnfgB shadow Register Default = 0x00	0xF1 R/W	Bit [2:0] Parallel Port DMA channel Select = 000 h/w jumpered 8-bit DMA (default) = 001 DMA channel 1 = 010 DMA channel 2 = 011 DMA channel 3 Bit [5:3] Parallel Port IRQ line Select = 000 h/w jumpered IRQ (default) = 001 IRQ 7 = 010 IRQ 9 = 011 IRQ 10 = 100 IRQ 11 = 101 IRQ 14 = 110 IRQ 15 = 111 IRQ 5 Bit [7:6] Reserved, ignores writes returns “0” on reads. The DMA/IRQ bits in this register are reflected in the Enhanced Parallel Port’s read only cnfgB register.	C

TABLE 221 - SERIAL PORT 1, LOGICAL DEVICE 4 [LOGICAL DEVICE NUMBER = 0X04]

NAME	REG INDEX	DEFINITION	STATE
Serial Port 1 Mode Register Default = 0x00	0xF0 R/W	Bit[0] MIDI Mode = 0 MIDI support disabled (default) = 1 MIDI support enabled Bit[1] High Speed = 0 High Speed Disabled (default) = 1 High Speed Enabled Bit[6:2] Reserved, set to “0” Bit[7] Reserved	C

TABLE 222 - INFRARED, LOGICAL DEVICE 5 [LOGICAL DEVICE NUMBER = 0X05]

NAME	REG INDEX	DEFINITION	STATE
Infrared Mode Register Default = 0x00	oxF0 R/W	Bit[0] MIDI Mode =0 MIDI support disabled (default) =1 MIDI support enabled Bit[1] High Speed =0 High Speed Disabled (default) =1 High Speed Enabled Bit[7:2] Reserved	C

NAME	REG INDEX	DEFINITION	STATE
IR Option Register Default = 0x00 This register sets the IR options and uses the same bit definitions as the FDC37C93x	oxF1 R/W	Bit[0] Receive Polarity =0 Active High =1 Active Low (default) Bit[1] Transmit Polarity =0 Active High (Default) =1 Active Low Bit[2] Duplex Select =0 Full Duplex (Default) =1 Half Duplex Bit[5:3] UART/IR Mode =000 Standard COMM (default) =001 IrDA SIR-A =010 ASK-IR =011 (IrDA SIR-B) =100 (IrDA HDLC) =101 (IrDA 4PPM) =110 (Consumer) =111 (Raw IR) Bit[7:6] IRCC 2.0 Output Mux =00 Active Device to COM-RX/COM-TX port (default) =01 Active Device to IRRX/IRTX port =10 Reserved-use AUX port not mapped to pins thus both IR and COM ports are inactive =11 Reserved, all ports are inactive	C

NAME	REG INDEX	DEFINITION	STATE
IR Half Duplex Timeout Default = 0x03	0xF2 R/W	Bit[7:0] These bits set the half duplex time-out for the IR port. This value is 0 to 10ms in 100µs increments =0x00 blank RX/TX during Transmit/Receive =0x01 blank TX/TX during Xmit/Rcv + 100µs ..... =0x64 blank RX/TX during Xmit/Rcv +10ms =0x65 - 0xFF : Reserved	

EN_1 : Bits [5:0] of the IR Option Configuration Register must be reconciled with bits[5:0] of the "SCE Configuration Register A" control register in the IRCC 2.0 Block, detailed in the IRCC 2.0 specification. Additionally bits [7:6] of the IR Option Configuration Register must be reconciled with bits[5:4] of the "SCE Configuration Register B" control register in the IRCC 2.0 Block. The last register written should update the information in both registers. Both sets of registers can use common latches to store the information.

TABLE 223 - RTC, LOGICAL DEVICE 6 [LOGICAL DEVICE NUMBER = 0X06]

NAME	REG INDEX	DEFINITION	STATE
RTC Mode Register Default = 0x00	0xF0 R/W	Bit[0] = 1 : Lock CMOS RAM 80-9Fh Bit[1] = 1 : Lock CMOS RAM A0-BFh Bit[2] = 1 : Lock CMOS RAM C0-DFh Bit[3] = 1 : Lock CMOS RAM E0-FEh Bit[7:4] Reserved, set to "0" Once set, bit[3:0] can not be cleared by a write; bits[3:0] are cleared on VCC2 Power On Reset, VCC2 Power Off, or upon a Hard Reset (nRESET_OUT asserted). Once lock bits are set, both the Host and the 8051 are locked out of accessing the locked locations as long as VCC1 and VCC2 are active. When VCC2 goes to 0V, the lock bits are cleared and the 8051 can access this RAM while nRESET_OUT is asserted.	C

NAME	REG INDEX	DEFINITION	STATE
RTC CMOS Bank 0 Index Register	OxF1 R	Shadowed RTC/CMOS Bank 0 Index Register	

TABLE 224 - KYBD, LOGICAL DEVICE 7 [LOGICAL DEVICE NUMBER = 0X07]

NAME	REG INDEX	DEFINITION	STATE
KRST_GA20	0xf0 R/W	Bit[0] : ENAB_P92 = 0 : Port 92 Disabled = 1 : Port 92 Enabled Bit[7:0] : Reserved, set to “0”.	

NOTE : Refer to the 8051 section for descriptions of these registers.

SYSTEM SHADOW REGISTERS

The FDC37N972 makes the following Control Registers readable by supplying a set of Index Registers accessable either through Logical Device 7 when in Configuration State or through the Open Mode Index and Data registers when in Run State.

	Sys. index	Sys R/W	8051 address (7F00+)	8051 R/W	Power Source	VCC1 POR	VCC2 POR	Zero Wait State (9)	Notes
Force Diskchange	MBX99	R	------	N/A	VCC2		03h		------
Floppy Data Rate Select Shadow Register	MBX9A	R	------	N/A	VCC2		N/A		------
UART1 FIFO Control Shadow Register	MBX9B	R	------	N/A	VCC2		00h		

FLOPPY DATA RATE SELECT SHADOW REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
8051 R/W	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
System R/W	R	R	R	R	R	R	R	R
Bit Def	Soft Reset	Power Down	0	PRE-COMP 2	PRE-COMP 1	PRE-COMP 0	Data Rate Select 1	Data Rate Select 0

Note: D1 and D0 are updated by a write to the Floppy Data Rate or CCR registers. Bits D7-D2 are updated by a write to the Floppy Data Rate register only.

FORCE DISKCHANGE

	D7-D2	D1	D0
System R/W	R	R/W	R/W
Bit Def	Reserved	1 = Force a diskchange indication when the DIR register (of the Floppy controller) is read, gated with Drive Select 0 or 1. These bits can be written to a "1" but are not clearable by the software. These bits are reset when nSTEP input is active with the proper drive select to the drive occurs. D0 is cleared on nSTEP and Drive Select 0; D1 is cleared on nSTEP and Drive Select 1.	

Equivalent logic: when read DIR bit 7 = (Drive_Sel_0 & D0) OR (Drive_Sel_1 & D1) OR DSK_CHG

ELECTRICAL SPECIFICATIONS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range..... 0^{o}C to $+70^{o}$C
Storage Temperature Range.....-55^{o} to $+150^{o}$C
Lead Temperature Range (soldering, 10 seconds) ..... $+325^{o}$C
Positive Voltage on any pin, with respect to Ground..... +5.5V
Negative Voltage on any pin, with respect to Ground..... -0.3V
Supply Voltage Range $V_{CC}1$ and $V_{CC}2$.....$V_{CC}1$ and $V_{CC}2$

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

TABLE 223 - OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc0	Vbat for RTC	2.4	3.0	3.3	V
Vcc1	Vcc for 8051	3.15	3.3	3.45	V
Vcc2	System Vcc	3.15	3.3	3.45	V
PCI_CLK	PCI Clock		33		MHz
XTAL1/XTAL2	RTC Crystal		32.768		kHz
CLOCKI	14.318 Clock Input		14.318		MHz

POWER COMSUMPTION IN VARIOUS STATES

V_{CC2} (VDC)	V_{CC1} (VDC)	8051 STATE	CLOCK STATE	SYM	TYP	MAX	COMMENTS
3.3	3.3	Run	24 MHz	I_{CC2} I_{CC1}	15 ma 24 ma	20 ma 30 ma	FLOPPY @ 1 Meg Data Rate I2C @ 24 MHz
3.3	3.3	Run	12 MHz	I_{CC2} I_{CC1}	13 ma 12 ma	15 ma 18 ma	Floppy @ 500K Data Rate I2C @ 12 MHz
3.3	3.3	Run	Ring OSC	I_{CC2} I_{CC1}	>1ma 8 ma	2 ma 10 ma	PLL On I2C Off
3.3	3.3	Idle	Ring OSC	I_{CC2} I_{CC1}	>1ma 5 ma	2 ma 7 ma	PLL Off
0	3.3	Run	Ring OSC	I_{CC2} I_{CC1}	 8 ma	 10 ma	PLL Off I2C Off
0	3.3	Idle	Ring OSC	I_{CC2} I_{CC1}	 6 ma	 8 ma	PLL Off I2C Off

V_{CC2} (VDC)	V_{CC1} (VDC)	8051 STATE	CLOCK STATE	SYM	TYP	MAX	COMMENTS
0	3.3	Sleep	Stop	I_{CC1}		160 µa	XOSEL=1
0	3.3	Sleep	Stop	I_{CC1}	5 µa	10 µa	XOSEL=0
0	0			I_{CC0}	40 µa	60 µa	2.4 < V_{cc0} < 4 VDC, XOSEL=1,
0	0			I_{CC0}	0.4 µa	1.5 µa	2.4 < V_{cc0} < 4 VDC, XOSEL = 0

Note: When a single-ended 32.768kHz clock source is selected (see Section 32kHz Clock Input. The FDC37N972 uses the XOSEL pin to select either a 32.768kHz input clock or a 32.768kHz crystal to drive the Real Time Clock Interface (Table 2 - PIN FUNCTION DESCRIPTION). When XOSEL = '0', The RTC uses a 32.768kHz crystal connected between the XTAL1 and XTAL2 pins. When XOSEL = '1', the RTC is driven by a 32.768kHz single-ended clock source connected to the XTAL2 pin.

DC SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, $V_{CC}1$ and $V_{CC}2$= $V_{CC}1$ and $V_{CC}2$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	Schmitt Trigger
ISP Type Input Buffer with 90 µA weak pull-up						
Low Input Level	V_{ILIS}	2.2		0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}		250		V	
Schmitt Trigger Hysteresis	V_{HYS}				mV	Schmitt Trigger
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	3.0			V	
O_{CLK2} Crystal Oscillator Output I_{CLK2} Crystal Oscillator Input	Use a 32 kHz parallel resonant crystal oscillator. The load capacitors are seen by the crystal as two capacitors in series and should be approximately 2 times the Co of the actual crystal used (C1=2Co). For example, a 7.5pF crystal should use two 15pF capacitors for proper loading.					

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers except PWRGD & VCC1_PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{CC}
Input Current PWRGD	I_{OH}		75	150	µA	V_{IN} = 0
O4 Type Buffer						
Low Output Level	V_{OL}	2.4		0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}				V	I_{OH} = -2 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	V_{OL} = 4 mA
Output Leakage	I_{OH}	-10		+10	µA	I_{OH} = 0 to V_{CC}
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	V_{OL} = 8 mA
Output Leakage	I_{OH}	-10		+10	µA	I_{OH} = 0 to V_{CC}
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -50 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 2)
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 2)
Input Leakage (All I and IS buffers except FAD[7:0]						
FAD[7:0] Input Leakage						
Low Input Leakage	I_{IL}	-100		+100	nA	V_{IN} = 0
High Input Leakage	I_{IH}	-100		+100	nA	V_{IN} = V_{CC}
IOD8 Type Buffer						
Low Output Level	V_{OL}	0.5			V	I_{OL}=8 mA
High Input Level	V_{IH}	2.0			V	
High Inputt Level	V_{IL}	0.8			V	
Output Leakage						
IOD16 Type Buffer						
Low Output Level	V_{OL}	0.5			V	I_{OL}=16 mA
High Input Level	V_{IH}	2.0			V	
High Inputt Level	V_{IL}	0.8			V	
Output Leakage						

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 2)
IP Type Buffer						
Low Input Level	V_{ILI}			0.8	V	
High Input Level	V_{IHI}	2.0			V	
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 2)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
PCI_CLK Type Buffer						See Specification for PCI Systems Version 6.0
PCI_IO Type Buffer						See Specification for PCI Systems Version 6.0
PCI_OD Type Buffer						See Specification for PCI Systems Version 6.0
ICLK Type Buffer Low Input Level High Input Level	 V_{ILI} V_{IHCLK}	 2.4		 0.4 	 V V	
ICLK2 Type Buffer **OCLK2 Type Buffer**	Use a 32 Khz parellel rosinant cystal oscillator. The load copacitors are seen by the crystal as tow capacitors in series and should be approximately 2 times the C_0 of the actual crystal used (c1- c_o.) For example a 7.5 pF cyrstal should use two 15 pF capacitors for proper loading.					
Supply Current Active Supply Current Sleep	I_{CC} I_{SLP}			50 25	mA µA	I_{CC2} + I_{CC1} (Note 1) I_{CC1} with V_{cc2} Off, Sleep mode

Notes:
1) This value is with the FDC at less than 2 MHz, and the 8051running at the ring oscillator drawing 8mA. The max value is 60mA with the FDC at 2 MHz. The ring oscillator is typically 4 – 8 MHz.
2) All output leakage's are measured with the current pins in high impedance

AC SPECIFICATIONS

AC TEST CONDITIONS

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{cc} = 5V

		LIMITS				
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**TEST CONDITION**
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS

LOAD CAPACITANCE

For the timing diagrams shown, the following capacitive loads are used.

TABLE 226 - CAPACITIVE LOADING

NAME	CAPACITANCE TOTAL (pF)	NAME	CAPACITANCE TOTAL (pF)
SD[0:7]	240	EMCLK	240
IOCHRDY	240	EMDAT	240
nIRQ8	120	IMCLK	240
nSMI	120	IMDAT	240
DRQ[0:1]	120	KBDAT	240
32kHz_OUT	50	KBCLK	240
24MHz_OUT	50	PS2DAT	240
nWGATE	240	PS2CLK	240
nWDATA	240	nNOWS	240
nHDSEL	240	FAD[0:7]	100
nDIR	240	FA[8:17]	100
nSTEP	240	nFRD	50
nDS[1:0]	240	nFWR	50
nMTR[1:0]	240	FALE	50
DRVDEN[1:0]	240	KSO[0:13]	100
TXD1	100	SIRQ	150
nRTS1	100	FPD	50
nDTR1	100	AB_DATA	100
PD[0:7]	240	AB_CLK	100
nSLCTIN	240	IRTX	50
nINIT	240	PWM[0:1]	50
nALF	240	nRESET_OUT	240
nSTROBE	240		

FAST GATEA20 IOW TIMING

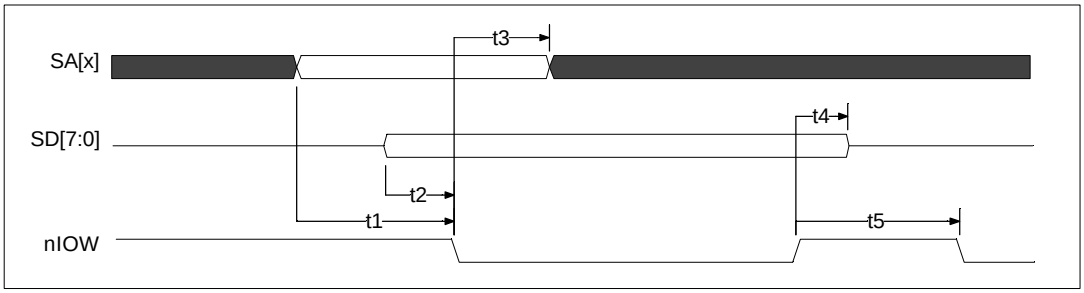


FIGURE 51 - FAST GATEA20 IOW TIMING

In order to use the FastGATEA20 speed-up mechanism, data must be available by the falling edge of nIOW.

TABLE 227 - FAST GATEA20 IOW TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SA[x] Valid to nIOW Asserted	10			ns
t2	SD[7:0] Valid to nIOW Asserted	0			ns
t3	nIOW Asserted to SA[x] Invalid	10			ns
t4	nIOW Deasserted to SD[7:0] Invalid	0			ns
t5	nIOW Deasserted to nIOW or nIOR Asserted	100			ns

ISA IO WRITE

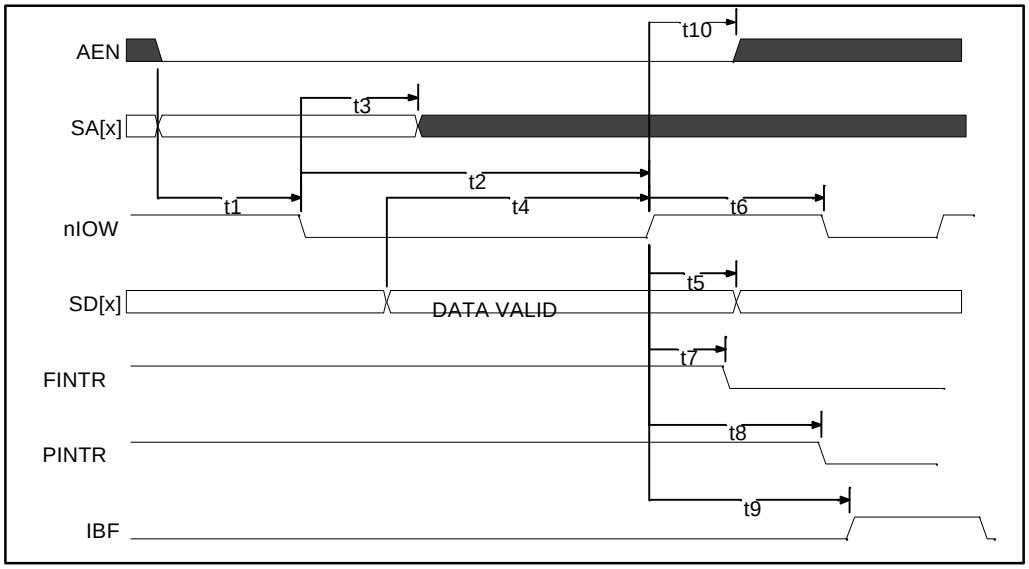


FIGURE 52 - ISA IO WRITE

TABLE 228 - ISA IO WRITE PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SA[x] and AEN Valid to nIOW Asserted	10			ns
t2	nIOW Asserted to nIOW Deasserted	80			ns
t3	nIOW Asserted to SA[x] Invalid	10			ns
t4	SD[x] Valid to nIOW Deasserted	45			ns
t5	SD[x] Hold from nIOW Deasserted	0			ns
t6	nIOW Deasserted to nIOW Asserted	25			ns
t7	nIOW Deasserted to FINTR Deasserted (Note 1)			55	ns
t8	nIOW Deasserted to PINTER Deasserted (Note 2)			260	ns
t9	IBF (internal signal) Asserted from nIOW Deasserted			40	ns
t10	nIOW Deasserted to AEN Invalid	10			ns

Note 1: FINTR refers to the IRQ used by the floppy disk logical device.
Note 2: PINTR refers to the IRQ used by the parallel port logical device.

ISA IO READ CYCLE

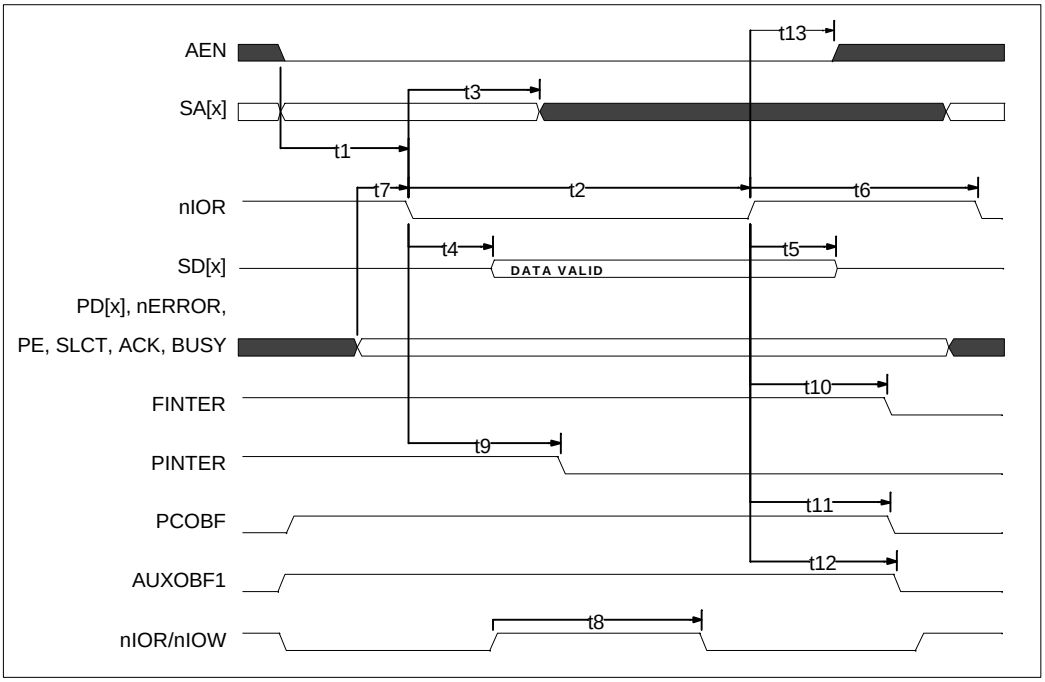


FIGURE 53 - ISA IO READ CYCLE

TABLE 229 - ISA IO READ TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SA[x] and AEN Valid to nIOR Asserted	10			ns
t2	nIOR Asserted to nIOR Deasserted	50			ns
t3	nIOR Asserted to SA[x] Invalid	10			ns
t4	nIOR Asserted to Data Valid			50	ns
t5	Data Hold/Float from nIOR Deasserted	10		25	ns
t6	nIOR Deasserted to nIOR Asserted	25			ns
t8	nIOR Asserted after nIOW Deasserted	80			ns
t8	nIOR/nIOR, nIOW/nIOW Transfers from/to ECP FIFO	150			ns
t7	Parallel Port Setup to nIOR Asserted			20	ns
t9	nIOR Asserted to PINTER Deasserted			55	ns
t10	nIOR Deasserted to FINTER Deasserted			260	ns
t11	nIOR Deasserted to PCOBF Deasserted (Notes 3,5)			80	ns

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t12	nIOR Deasserted to AUXOBF1 Deasserted (Notes 4,5)			80	ns
t13	nIOR Deasserted to AEN Invalid	10			ns

Note 1: FINTR refers to the IRQ used by the floppy disk.
Note 2: PINTR refers to the IRQ used by the parallel port.
Note 3: PCOBF is used for the Keyboard IRQ.
Note 4: AUXOBF1 is used for the Mouse IRQ.
Note 5: Applies only if deassertion is performed in hardware.

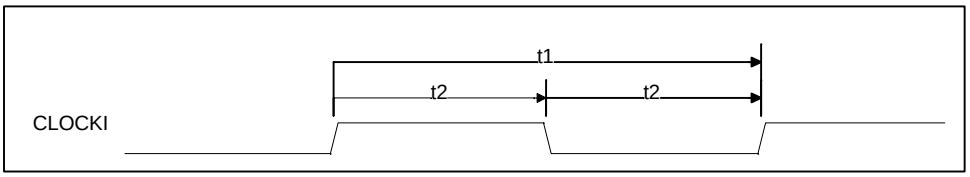


FIGURE 54 - INPUT CLOCK TIMING

TABLE 230 - INPUT CLOCK TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318 MHz (Note)		69.84		ns
t2	Clock High Time/Low Time for 14.318 MHz	15			ns
t_r, t_f	Clock Rise Time/Fall Time (not shown)			5	ns

Note: Tolerance is ± 0.01%.

DMA TIMING (SINGLE TRANSFER MODE)

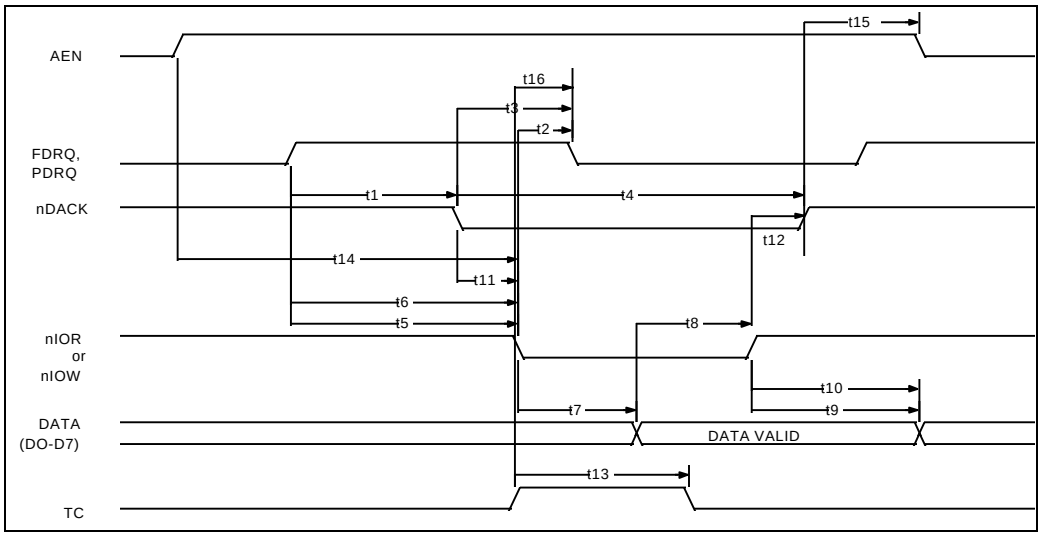


FIGURE 55 - DMA TIMING (SINGLE TRANSFER MODE)

TABLE 231 - DMA TIMING (SINGLE TRANSFER MODE) PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDACK Delay Time from FDRQ High	0			ns
t2	DRQ Reset Delay from nIOR or nIOW			100	ns
t3	FDRQ Reset Delay from nDACK Low			100	ns
t4	nDACK Width	150			ns
t5	nIOR Delay from FDRQ High	0			ns
t6	nIOW Delay from FDRQ High	0			ns
t7	Data Access Time from nIOR Low			100	ns
t8	Data Set Up Time to nIOW High	40			ns
t9	Data to Float Delay from nIOR High	10		60	ns
t10	Data Hold Time from nIOW High	10			ns
t11	nDACK Set Up to nIOW/nIOR Low	5			ns
t12	nDACK Hold after nIOW/nIOR High	10			ns
t13	TC Pulse Width	60			ns
t14	AEN Set Up to nIOR/nIOW	40			ns
t15	AEN Hold from nDACK	10			ns
t16	TC Active to PDRQ Inactive			100	ns

DMA TIMING (BURST TRANSFER MODE)

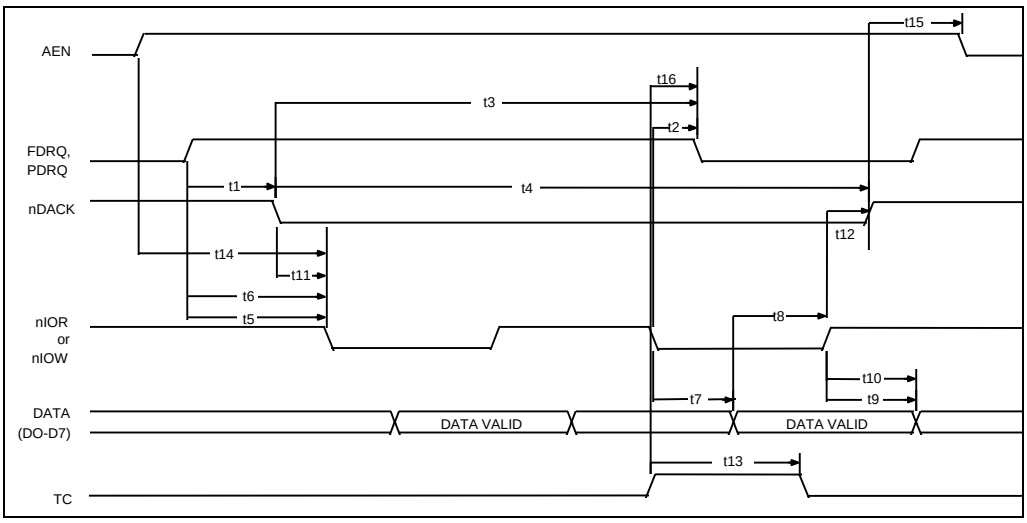


FIGURE 56 - DMA TIMING (BURST TRANSFER MODE)

TABLE 232 - DMA TIMING (BURST TRANSFER MODE) PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDACK Delay Time from FDRQ High	0			ns
t2	DRQ Reset Delay from nIOR or nIOW			100	ns
t3	FDRQ Reset Delay from nDACK Low			100	ns
t4	nDACK Width	150			ns
t5	nIOR Delay from FDRQ High	0			ns
t6	nIOW Delay from FDRQ High	0			ns
t7	Data Access Time from nIOR Low			100	ns
t8	Data Set Up Time to nIOW High	40			ns
t9	Data to Float Delay from nIOR High	10		60	ns
t10	Data Hold Time from nIOW High	10			ns
t11	nDACK Set Up to nIOW/nIOR Low	5			ns
t12	nDACK Hold after nIOW/nIOR High	10			ns
t13	TC Pulse Width	60			ns
t14	AEN SET UP TO NIOR/NIOW	40			ns
t15	AEN Hold from nDACK	10			ns
t16	TC Active to PDRQ Inactive			100	ns

FLOPPY DISK DRIVE TIMING (AT MODE)

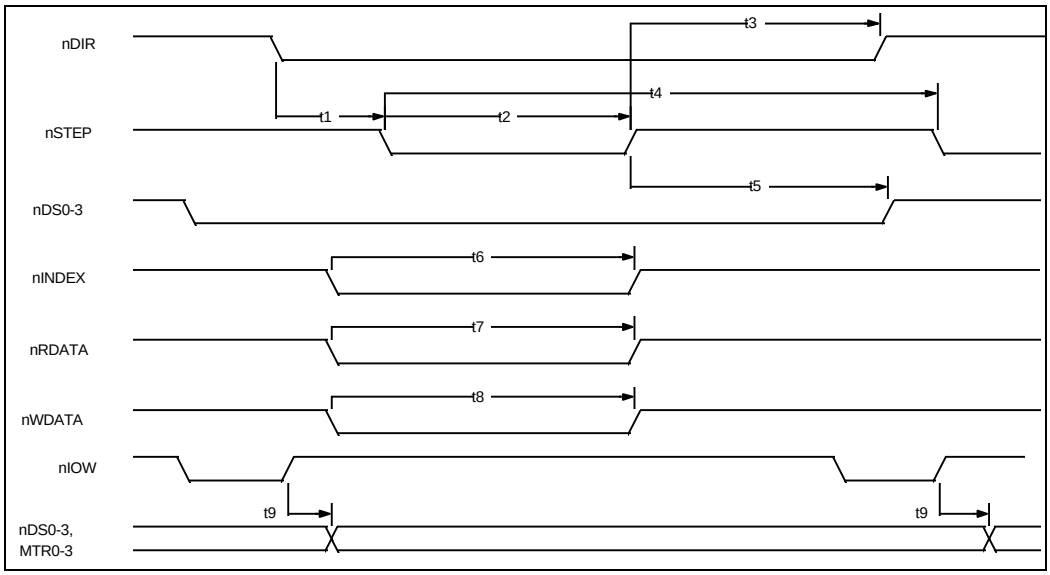


FIGURE 57 - FLOPPY DISK DRIVE TIMING (AT MODE)

TABLE 233 - FLOPPY DISK DRIVE TIMING (AT MODE) PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-3 Hold Time from nSTEP high		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-3, MTRO-3 from End of nIOW		25		ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = Controller Clock to FDC
WCLK = 2 x Data Rate

SERIAL PORT TIMING

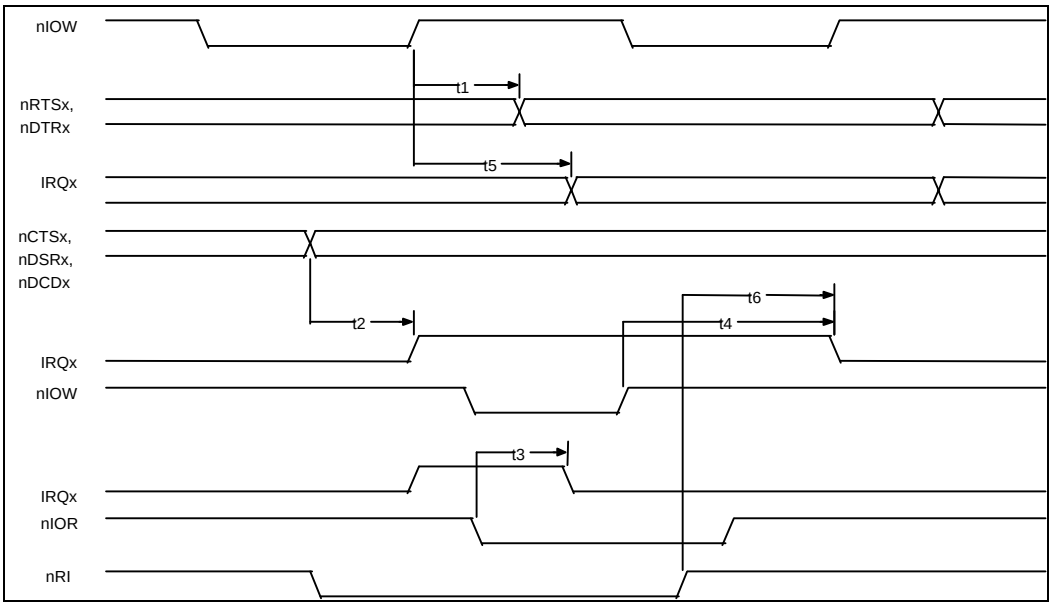


FIGURE 58 - SERIAL PORT TIMING

TABLE 234 - SERIAL PORT TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nRTSx, nDTRx Delay from nIOW			200	ns
t2	IRQx Active Delay from nCTSx, nDSRx, nDCDx			100	ns
t3	IRQx Inactive Delay from nIOR (Leading Edge)			120	ns
t4	IRQx Inactive Delay from nIOW (Trailing Edge)			125	ns
t5	IRQx Inactive Delay from nIOW	10		100	ns
t6	IRQx Active Delay from 0x			100	ns

PARALLEL PORT TIMING

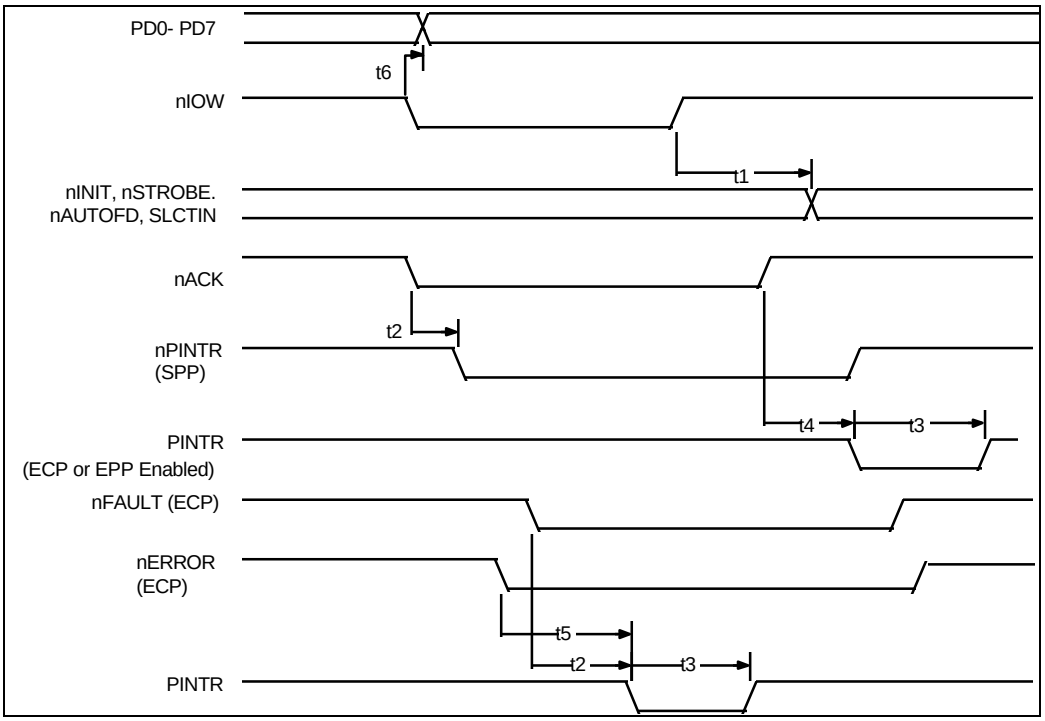


FIGURE 59 - PARALLEL PORT TIMING

TABLE 235 - PARALLEL PORT TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PD0-7, nINIT, nSTROBE, nALF Delay from nIOW			100	ns
t2	PINTR Delay from nACK, nFAULT			60	ns
t3	PINTR Active Low in ECP and EPP Modes	200		300	ns
t4	PINTR Delay from nACK			105	ns
t5	nERROR Active to PINTR Active			105	ns
t6	PD0 - PD7 Delay from IOW Active			100	ns

EPP 1.9 DATA OR ADDRESS WRITE CYCLE

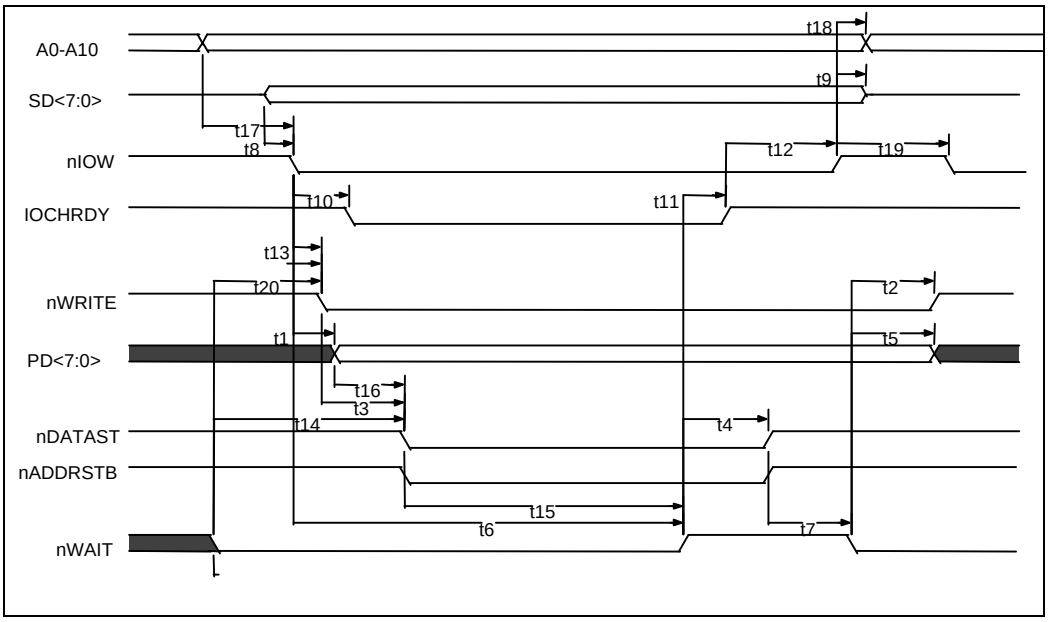


FIGURE 60 - EPP 1.9 DATA OR ADDRESS WRITE CYCLE

TABLE 236 - EPP 1.9 DATA OR ADDRESS WRITE PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nIOW Asserted to PDATA Valid	0		50	ns
t2	nWAIT Asserted to nWRITE Change (Note 1)	60		185	ns
t3	nWRITE to Command Asserted	5		35	ns
t4	nWAIT Deasserted to Command Deasserted (Note 1)	60		190	ns
t5	nWAIT Asserted to PDATA Invalid (Note 1)	0			ns
t6	Time Out	10		12	µs
t7	Command Deasserted to nWAIT Asserted	0			ns
t8	SDATA Valid to nIOW Asserted	10			ns
t9	nIOW Deasserted to DATA Invalid	0			ns
t10	nIOW Asserted to IOCHRDY deasserted	0		24	ns
t11	nWAIT Deasserted to IOCHRDY Asserted (Note 1)	60		160	ns
t12	IOCHRDY Asserted to nIOW Deasserted	10			ns
t13	nIOW Asserted to nWRITE Asserted	0		70	ns
t14	nWAIT Asserted to Command Asserted (Note 1)	60		210	ns
t15	Command Asserted to nWAIT Deasserted	0		10	µs
t16	PDATA Valid to Command Asserted	10			ns

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t17	Ax Valid to nIOW Asserted	40			ns
T18	nIOW Deasserted to Ax Invalid	10			ns
t19	nIOW Deasserted to nIOW or nIOR Asserted	40			ns
t20	nWAIT Asserted to nWRITE Asserted (Note 1)	60		185	ns

Note 1: nWAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

EPP 1.9 DATA OR ADDRESS READ CYCLE

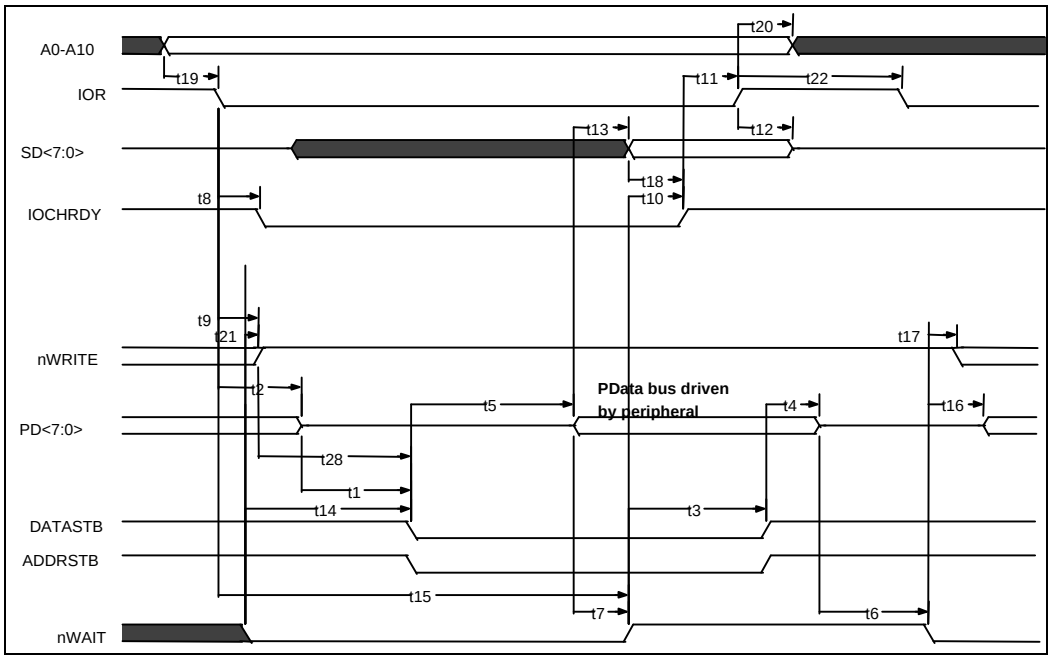


FIGURE 61 - EPP 1.9 DATA OR ADDRESS READ CYCLE

TABLE 237 - EPP 1.9 DATA OR ADDRESS READ CYCLE TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA HI-Z TO COMMAND ASSERTED	0		30	ns
t2	nIOR Asserted to PDATA Hi-Z	0		50	ns
t3	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t4	Command Deasserted to PDATA Hi-Z	0			ns
t5	Command Asserted to PDATA Valid	0			ns
t6	PDATA Hi-Z to nWAIT Deasserted	0			µs
t7	PDATA Valid to nWAIT Deasserted	0			ns
t8	nIOR Asserted to IOCHRDY Deasserted	0		24	ns
t9	nWRITE Deasserted to nIOR Asserted (Note 2)	0			ns
t10	nWAIT Deasserted to IOCHRDY Asserted (Note 1)	60		160	ns
t11	IOCHRDY Asserted to nIOR Deasserted	0			ns
t12	nIOR Deasserted to SDATA Hi-Z (Hold Time)	0		40	ns
t13	PDATA Valid to SDATA Valid	0		75	ns
t14	nWAIT Asserted to Command Asserted	0		195	ns

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t15	Time Out	10		12	µs
t16	nWAIT Deasserted to PDATA Driven (Note 1)	60		190	ns
t17	nWAIT Deasserted to nWRITE Modified (Notes 1,2)	60		190	ns
t18	SDATA Valid to IOCHRDY Deasserted (Note 3)	0		85	ns
t19	Ax Valid to nIOR Asserted	40			ns
t20	nIOR Deasserted to Ax Invalid	10		10	ns
t21	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t22	nIOR Deasserted to nIOW or nIOR Asserted	40			ns
t28	nWRITE Deasserted to Command	1			ns

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
Note 2: When not executing a write cycle, EPP nWRITE is inactive high.
Note 3: 85 is true only if t7 = 0.

EPP 1.7 DATA OR ADDRESS WRITE CYCLE

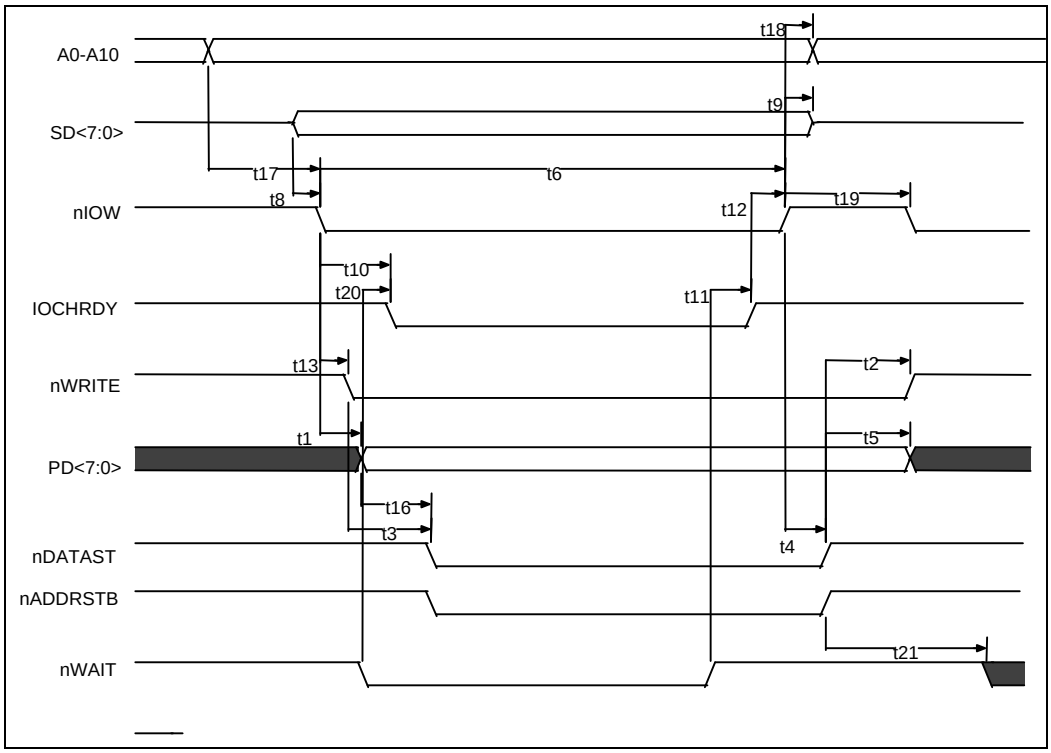


FIGURE 62 - EPP 1.7 DATA OR ADDRESS WRITE CYCLE

TABLE 238 - EPP 1.7 DATA OR ADDRESS WRITE CYCLE TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nIOW Asserted to PDATA Valid	0		50	ns
t2	Command Deasserted to nWRITE Change	0		40	ns
t3	nWRITE to Command	5		35	ns
t4	nIOW Deasserted to Command Deasserted (Note 2)			50	ns
t5	Command Deasserted to PDATA Invalid	50			ns
t6	Time Out	10		12	µs
t8	SDATA Valid to nIOW Asserted	10			ns
t9	nIOW Deasserted to DATA Invalid	0			ns
t10	nIOW Asserted to IOCHRDY deasserted	0		24	ns
t11	nWAIT Deasserted to IOCHRDY Asserted			40	ns
t12	IOCHRDY Asserted to nIOW Deasserted	10			ns

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t13	nIOW Asserted to nWRITE Asserted	0		50	ns
t16	PDATA Valid to Command Asserted	10		35	ns
t17	Ax Valid to nIOW Asserted	40			ns
t18	nIOW Deasserted to Ax Invalid	10			µs
t19	nIOW Deasserted to nIOW or nIOR Asserted	100			ns
t20	nWAIT Asserted to IOCHRDY Asserted			45	ns
t21	Command Deasserted to nWAIT Deasserted	0			ns

Note 1: nWRITE is controlled by clearing the PDIR bit to "0" in the control register before performing an EPP Write.

Note 2: The number is only valid if nWAIT is active when IOW goes active.

EPP 1.7 DATA OR ADDRESS READ CYCLE

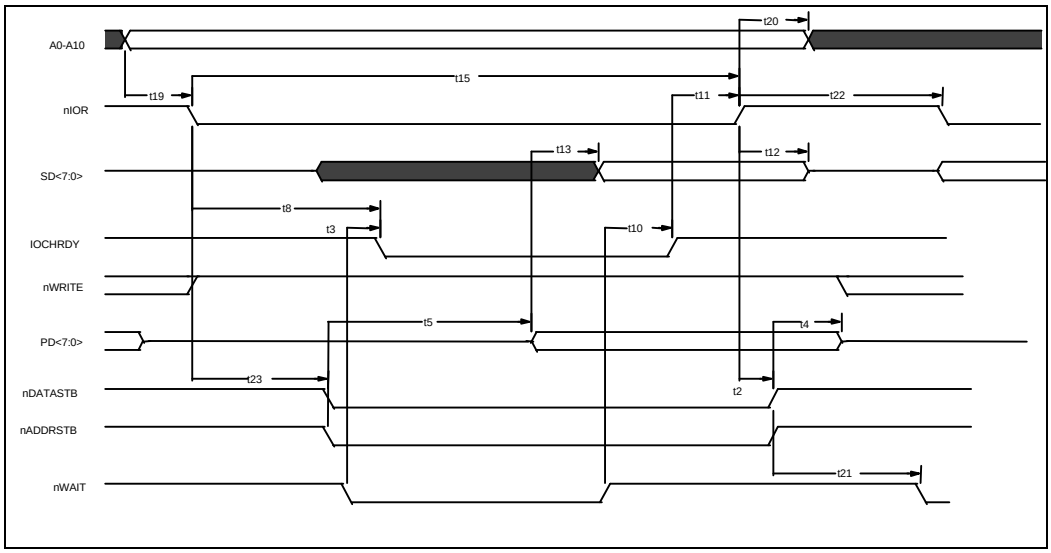


FIGURE 63 - EPP 1.7 DATA OR ADDRESS READ CYCLE

TABLE 239 - EPP 1.7 DATA OR ADDRESS READ CYCLE TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t2	nIOR Deasserted to Command Deasserted			50	ns
t3	nWAIT Asserted to IOCHRDY Deasserted	0		40	ns
t4	Command Deasserted to PDATA Hi-Z	0			ns
t5	Command Asserted to PDATA Valid	0			ns
t8	nIOR Asserted to IOCHRDY Asserted			24	ns
t10	nWAIT Deasserted to IOCHRDY Deasserted			50	ns
t11	IOCHRDY Deasserted to nIOR Asserted	0			ns
t12	nIOR Deasserted to SDATA High-Z (Hold Time)	0		40	ns
t13	PDATA Valid to SDATA Valid			40	ns
t15	Time Out	10		12	µs
t19	Ax Valid to nIOR Asserted	40			ns
t20	nIOR Deasserted to Ax Invalid	10			ns
t21	Command Deasserted to nWAIT Deasserted	0			ns
t22	nIOR Deasserted to nIOW or nIOR Asserted	40			ns
t23	nIOR Asserted to Command Asserted			55	ns

Note: WRITE is controlled by setting the PDIR bit to "1" in the control register before performing an EPP Read.

ECP PARALLEL PORT TIMING

PARALLEL PORT FIFO (MODE 101)

The standard parallel port is run at or near the peak 500Kbytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK, but begins the next transfer based on Busy. Refer to FIGURE 55.

ECP PARALLEL PORT TIMING

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft. cable. If a shorter cable is used then the bandwidth will increase.

FORWARD-IDLE

When the host has no data to send it keeps HostClk () high and the peripheral will leave PeriphClk (Busy) low.

FORWARD DATA TRANSFER PHASE

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nSTROBE) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nSTROBE) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in FIGURE 59. The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nSTROBE).

REVERSE-IDLE PHASE

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

REVERSE DATA TRANSFER PHASE

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready it to accept a byte it sets HostAck (nALF) high to acknowledge the handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data it sets HostAck (nALF) low, completing the transfer. This sequence is shown in FIGURE 57 - FLOPPY DISK DRIVE TIMING (AT MODE)

OUTPUT DRIVERS

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-collector), the drivers are dynamically changed from open-collector to totem-pole. The timing for the dynamic driver change is specified in the IEEE 1284 Extended Capabilities Port Protocol and ISA

Interface Standard, Rev. 1.14, July 14, 1996, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

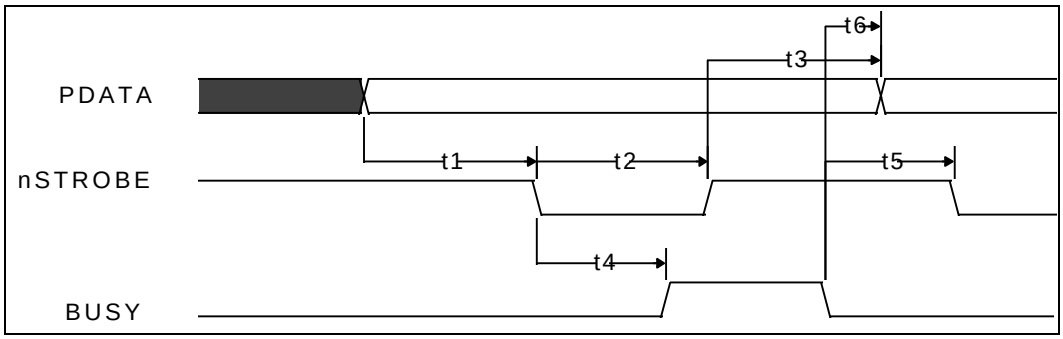


FIGURE 64 - PARALLEL PORT FIFO TIMING

TABLE 240 - PARALLEL PORT FIFO TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	DATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	DATA Hold from nSTROBE Inactive (Note 1)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (Note 1)	80			ns

Note 1: The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

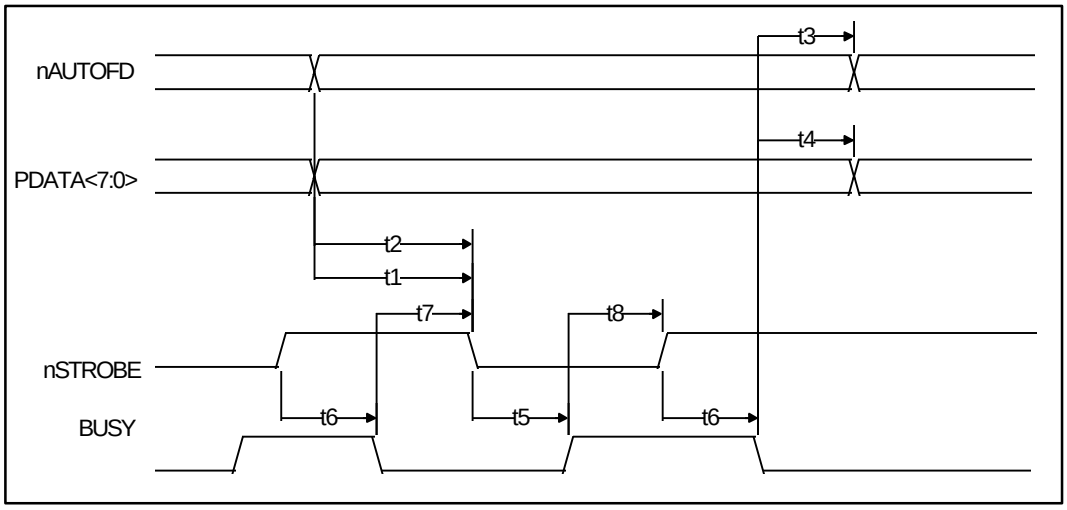


FIGURE 65 - ECP PARALLEL PORT FORWARD TIMING

TABLE 241 - ECP PARALLEL PORT FORWARD TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nALF Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nALF Changed (Notes 1,2)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (Notes 1,2)	80		180	ns
t5	nSTROBE Deasserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (Notes 1,2)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (Note 2)	80		180	ns

Note 1: Maximum value only applies if there is data in the FIFO waiting to be written out.
Note 2: BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

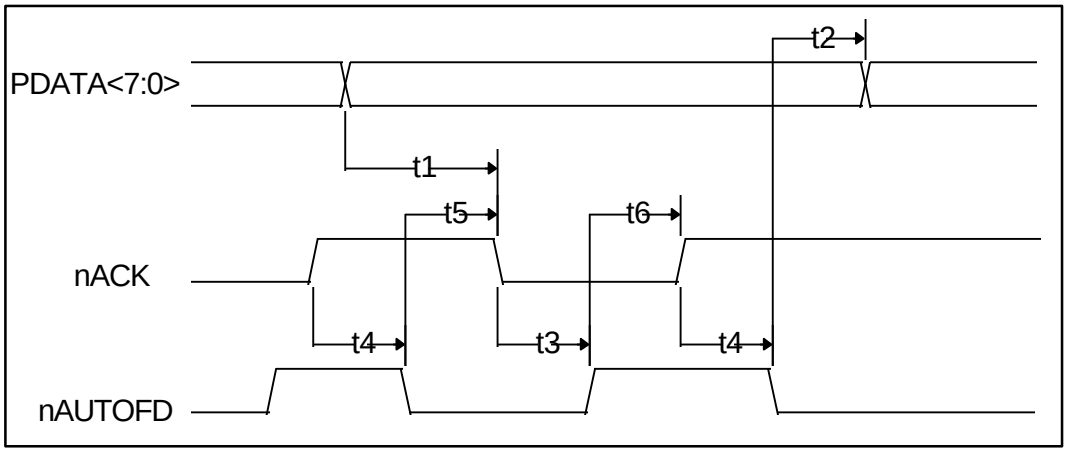


FIGURE 66 - ECP PARALLEL PORT REVERSE TIMING

TABLE 242 - ECP PARALLEL PORT REVERSE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nALF Deasserted to PDATA Changed	0			ns
t3	nACK Asserted to nALF Deasserted (Notes 1,2)	80		200	ns
t4	nACK Deasserted to nALF Asserted (Note 2)	80		200	ns
t5	nALF Asserted to nACK Asserted	0			ns
t6	nALF Deasserted to nACK Deasserted	0			ns

Note 1: Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nALF low.

Note 2: nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

ACCESS.BUS TIMING

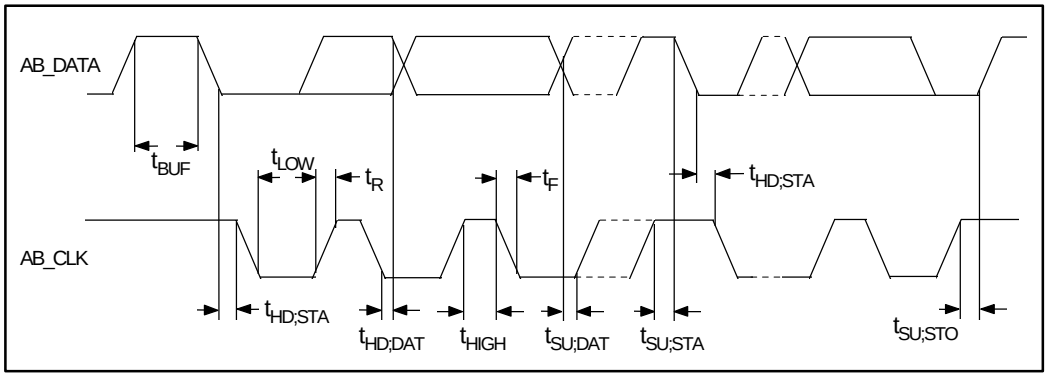


FIGURE 67 - ACCESS.BUS TIMING

TABLE 243 - ACCESS.BUS TIMING PARAMETERS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
f_{SCL}	SCL Clock Frequency			100	kHz
t_{BUF}	Bus Free Time	4.7			µs
$t_{SU;STA}$	START Condition Set-Up Time	4.7			µs
$t_{HD;STA}$	START Condition Hold Time	4.0			µs
t_{LOW}	SCL LOW Time	4.7			µs
t_{HIGH}	SCL HIGH Time	4.0			µs
t_R	SCL and SDA Rise Time			1.0	µs
t_F	SCL and SDA Fall Time			0.3	µs
$t_{SU;DAT}$	Data Set-Up Time	0.25			µs
$t_{HD;DAT}$	Data Hold Time	0			µs
$t_{SU;STO}$	STOP Condition Set-Up Time	4.0			µs

HOST FLASH READ TIMING

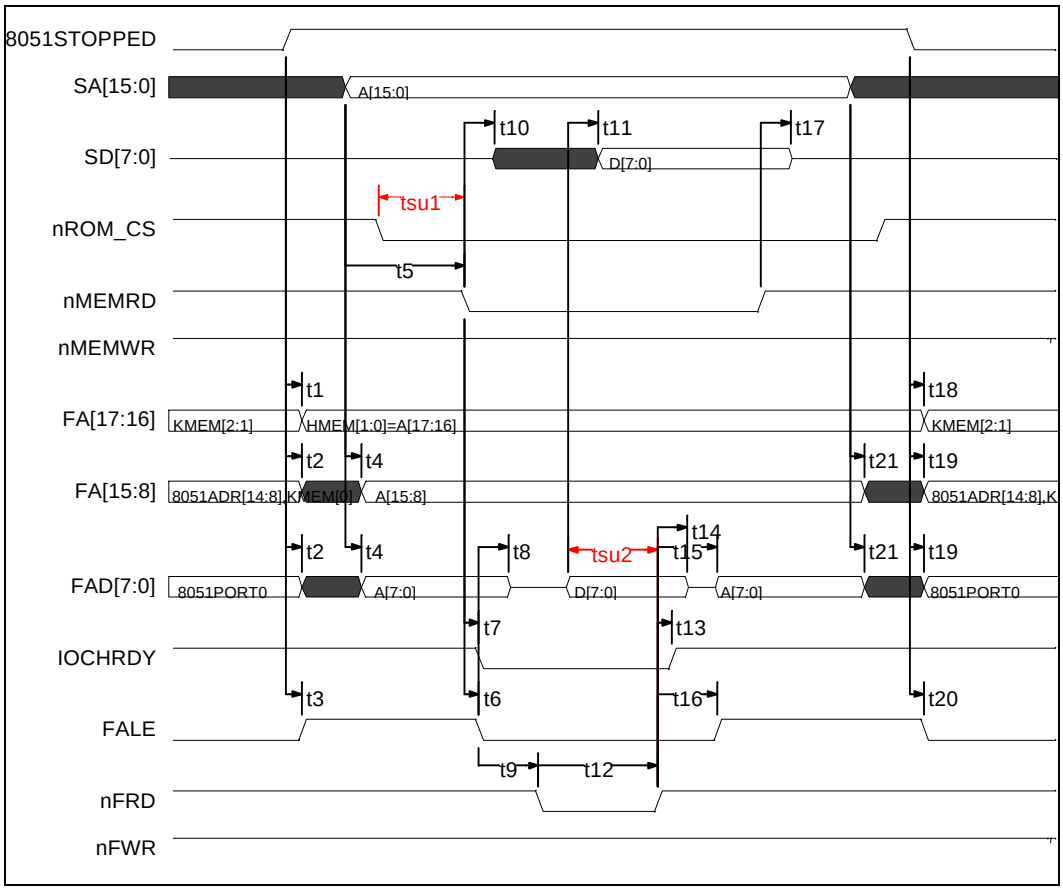


FIGURE 68 - HOST FLASH READ TIMING

TABLE 244 - HOST FLASH READ TIMING PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	8051 stopped condition met to FA[17:16] sourced by internal register HMEM[1:0]			40	ns
t2	8051 stopped condition met to FA[15:0] driven by SA[15:0]			40	ns
t3	8051 stopped condition met to FALE asserted			40	ns
t4	SA[15:0] valid to FA[15:0] valid propogation delay			40	ns
t5	SA[15:0] valid to nMEMRD asserted	88			ns
t6	nMEMRD asserted to FALE de-asserted	21		63	ns
t7	nMEMRD asserted to IOCHRDY de-asserted (Note1)			24	ns
t8	FALE de-asserted to FAD[7:0] tristated			42	ns
t9	FALE de-asserted to nFRD asserted			84	ns
t10	nMEMRD asserted to SD[7:0] driven			30	ns
t11	FAD[7:0] data valid to SD[7:0] data valid propogation delay			40	ns
t12	nFRD, Flash Read, asserted pulse width (Note2)	120 [3 sclk]		200 [5 sclk]	ns
t13	nFRD de-asserted to IOCHRDY asserted	0		20	ns
t14	FAD[7:0] Data hold time from nFRD de-asserted	0			ns
t15	SA[7:0] muxed onto FAD[7:0] following the de-assertion of nFRD			42	ns
t16	nFRD de-asserted to FALE asserted for next cycle			42	ns
t17	SD[7:0] data hold time from nMEMRD de-asserted	10			ns
t18	8051 clock started condition met to FA[17:16] sourced by internal register KMEM[2:1]			40	ns
t19	8051 clock started condition met to FA[15] sourced by KMEM[0] and FA[14:0] driven by the 8051			40	ns
t20	8051 clock started condition met to FALE de-asserted			40	ns
t21	SA[15:0] invalid to FA[15:0] invalid propagation delay			40	ns
tsu1	nROM_CS asserted to nMEMRD setup time	20			ns
tsu2	FAD[7:0] Data valid to nFRD de-asserted setup time	20			ns

Note 1: Systems designed prior to the EISA Specification, R3.12, which sample CHRDY on the rising edge of BCLK require that IOCHRDY is deasserted within 24 ns.

Note 2: The Flash Read signal pulse width is programmable through a configuration register, the time values shown are for an internal sclk=24 MHz derived from the 14.318 MHz input.

HOST FLASH READ/WRITE

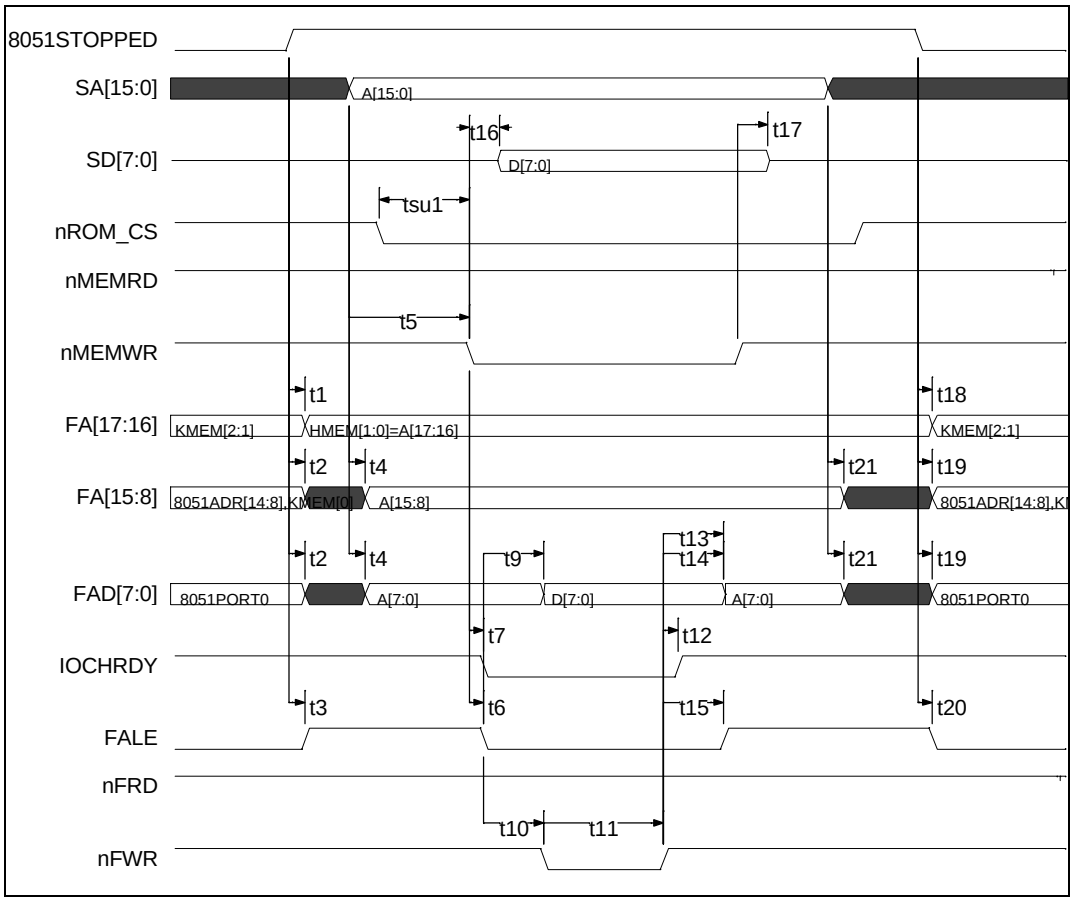


FIGURE 69 - HOST FLASH WRITE TIMING PARAMETERS

TABLE 245 - HOST FLASH WRITE TIMING PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	8051 stopped condition met to FA[17:16] sourced by internal register HMEM[2:1]			40	ns
t2	8051 stopped condition met to FA[15] driven by SA[15:0]			40	ns
t3	8051 stopped condition met to FALE asserted			40	ns
t4	SA[15:0] valid to FA[15:0] valid propogation delay			40	ns
t5	SA[15:0] valid to nMEMWR asserted	88			ns
t6	nMEMWR asserted to FALE de-asserted	21		63	ns
t7	nMEMWR asserted to IOCHRDY de-asserted (Note 1)			24	ns
t9	FALE de-asserted to SD[7:0] driven onto FAD[7:0]			42	ns
t10	FALE de-asserted to nFWR asserted			84	ns
t11	nFWR, Flash Write, asserted pulse width (Note 2)	120 [3 sclk]		200 [5 sclk]	ns
t12	nFWR de-asserted to IOCHRDY asserted			20	ns
t13	FAD[7:0] Data hold time from nFWR de-asserted			42	ns
t14	SA[7:0] muxed onto FAD[7:0] following the de-assertion of nFWR			42	ns
t15	nFWR deasserted to FALE asserted for next cycle			42	ns
t16	nMEMWR asserted to SD[7:0] valid			-10	ns
t17	SD[7:0] data hold time from nMEMWR de-asserted	10			ns
t18	8051 clock started condition met to FA[17:16] sourced by internal register KMEM[2:1]			40	ns
t19	8051 clock started condition met to FA[15] sourced by KMEM[0] and FA[14:0] driven by the 8051			40	ns
t20	8051 clock started condition met to FALE de-asserted			40	ns
t21	SA[15:0] invalid to FA[15:0] invalid propagation delay			40	ns
tsu1	nROM_CS asserted to nMEMWR setup time	20			ns

Note 1: Systems designed prior to the EISA Specification, R3.12, which sample CHRDY on the rising edge of BCLK require that IOCHRDY is deasserted within 24 ns.

Note 2: The Flash Write signal pulse width is programmable through a configuration register, the time values shown are for an internal sclk=24 MHz derived from the 14.318 MHz input

ZERO WAIT STATE (NOWS) TIMING

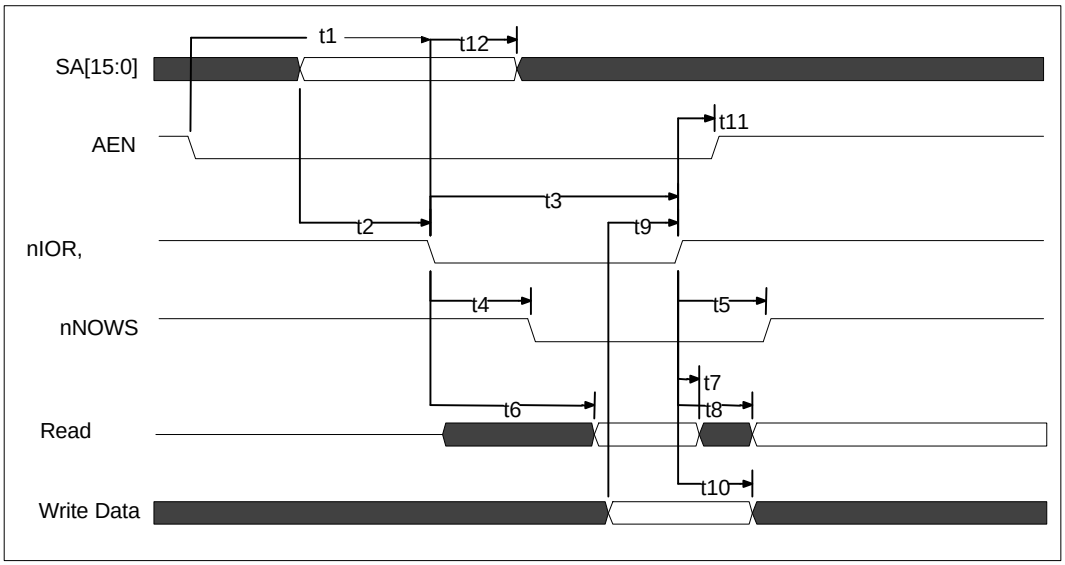


FIGURE 70 - ZERO WAIT STATE (NOWS) TIMING

TABLE 246 - ZERO WAIT-STATE TIMING PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	AEN Valid Before nIOR, nIOW Asserted	10			ns
t2	SA[15:0] Valid Before nIOR Asserted	10			ns
t3	nIOR, nIOW Pulse Width	80			ns
t4	nIOR, nIOW Asserted to nNOWS Asserted			50	ns
t5	nIOR, nIOW Negated to nNOWS Floated			35	ns
t6	nIOR Asserted to Read Data Valid			50	ns
t7	nIOR Negated to Read Data Invalid (Hold Time)	0			ns
t8	nIOR Negated to Data Bus Floated			24	ns
t9	Write Data Valid Before nIOW Deasserted	45			ns
t10	nIOW Negated to Write Data Invalid (Hold Time)	0			ns
t11	nIOR, nIOW Negated to AEN Invalid	10			ns
t12	nIOR, nIOW Negated to SA[15:0] Invalid	10			ns

FLASH PROGRAM FETCH TIMING

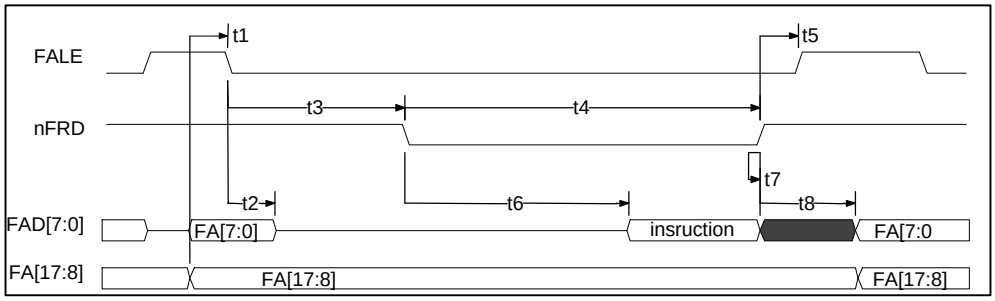


FIGURE 71 - 8051 FLASH PROGRAM FETCH TIMING

TABLE 247 - 8051 FLASH PROGRAM FETCH TIMING PARAMETERS

8051 Clock = 12 MHz					
	PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
t1	Address Valid to FALE Low	38	41		ns
t2	Address Hold Following FALE Low	35	60		ns
t3	FALE Low to nFRD Low	35	45	50	ns
t4	nFRD Pulse Width	150	162		ns
t5	nFRD High to FALE High	0	5	10	ns
t6	nFRD Low to Valid Instruction			135	ns
t7	Instruction Hold Following nFRD	0			ns
t8	Instruction Float Following nFRD			80	ns
8051 Clock = 24 MHz					
	PARAMETER @24 MHz	**MIN**	**TYP**	**MAX**	**UNITS**
t1	Address Valid to FALE Low	15	20		ns
t2	Address Hold Following FALE Low	35	40		ns
t3	FALE Low to nFRD Low	18	23	30	ns
t4	nFRD Pulse Width	60	82		ns
t5	nFRD High to FALE High	0	6	10	ns
t6	nFRD Low to Valid Instruction In			40	ns
t7	Instruction Hold Following nFRD	0			ns
t8	Instruction Float Following nFRD			40	ns

Min and Max delays shown for an 8051 clock of 12 MHz and 24 MHz as indicated. Device Mode Register bits [1:0] = 00 (See Global Configuration Registers, Table 214, address 0x25).

8051 FLASH READ TIMING

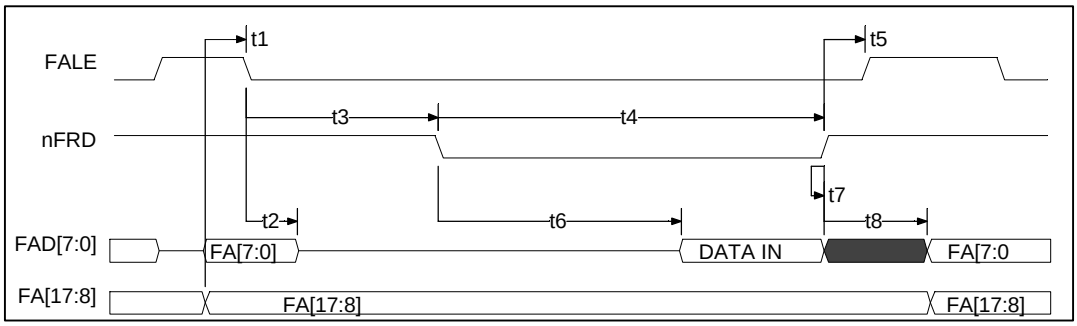


FIGURE 72 - 8051 FLASH READ TIMIING

TABLE 248 - FLASH READ TIMIING PARAMETERS

8051 Clock = 12 MHz					
	PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
t1	Address Valid to FALE Low	38	41		ns
t2	Address Hold Following FALE Low	35	60		ns
t3	FALE Low to nFRD Low	35	45	50	ns
t4	nFRD Pulse Width	150	162		ns
t5	nFRD High to FALE High	0	5	10	ns
t6	nFRD Low to Valid Data In			135	ns
t7	Data Hold Following nFRD	0			ns
t8	Data Float Following nFRD			80	ns
8051 Clock =24 MHz					
	PARAMETER @24 MHz	**MIN**	**TYP**	**MAX**	**UNITS**
t1	Address Valid to FALE Low	15	20		ns
t2	Address Hold Following FALE Low	35	40		ns
t3	FALE Low to nFRD Low	18	23	30	ns
t4	nFRD Pulse Width	60	82		ns
t5	nFRD High to FALE High	0	6	10	ns
t6	nFRD Low to Valid Data In			40	ns
t7	Data Hold Following nFRD	0			ns
t8	Data Float Following nFRD			40	ns

Min and Max delays shown for an 8051 clock of 12 MHz and 24 MHz as indicated. Device Mode Register bits [1:0] = 00 (See Global Configuration Registers, Table 214, address 0x25).

8051 FLASH WRITE TIMING

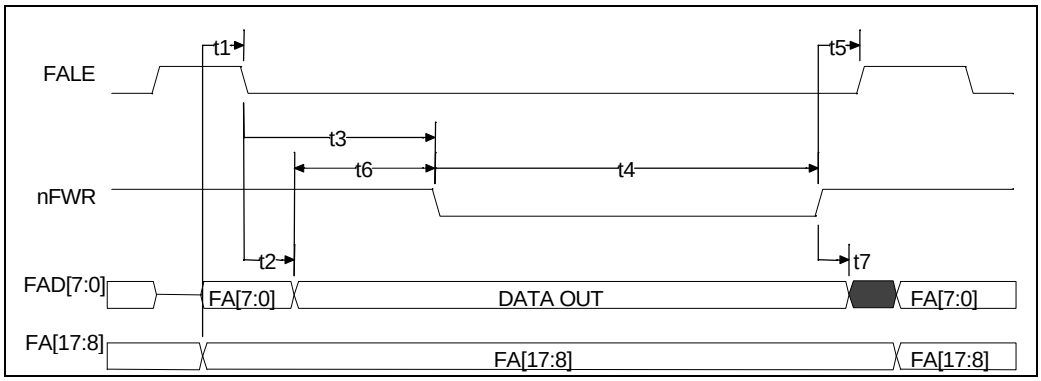


FIGURE 73 - 8051 FLASH WRITE TIMING

TABLE 249 - FLASH WRITE TIMING PARAMETERS

8051 Clock = 12 MHz					
	PARAMETER @12MHz	**MIN**	**TYP**	**MAX**	**UNITS**
t1	Address Valid to FALE Low	38	42		ns
t2	Address Hold Following FALE Low	38	41		ns
t3	FALE Low to nFWR Low	110	124	140	ns
t4	nFWR Pulse Width	300	332		ns
t5	nFWR High to FALE High	70	85	100	ns
t6	Data Valid to nFWR Falling Edge	70	84		ns
t7	Data Hold Following nFWR	150	172		ns
8051 Clock =24 MHz					
	PARAMETER @ 24 MHz	**MIN**	**TYP**	**MAX**	**UNITS**
t1	Address Valid to FALE Low	14	20		ns
t2	Address Hold Following FALE Low	18	22		ns
t3	FALE Low to nFWR Low	48	62	76	ns
t4	nFWR Pulse Width	130	162		ns
t5	nFWR High to FALE High	40	50	60	ns
t6	Data Valid to nFWR Falling Edge	30	41		ns
t7	Data Hold Following nFWR	60	84		ns

Min and Max delays shown for an 8051 clock of 12 MHz and 24 MHz as indicated. Device Mode Register bits [1:0] = 00 (See Global Configuration Registers, Table 214, address 0x25).

PS/2 CHANNEL RECEIVE TIMING DIAGRAM

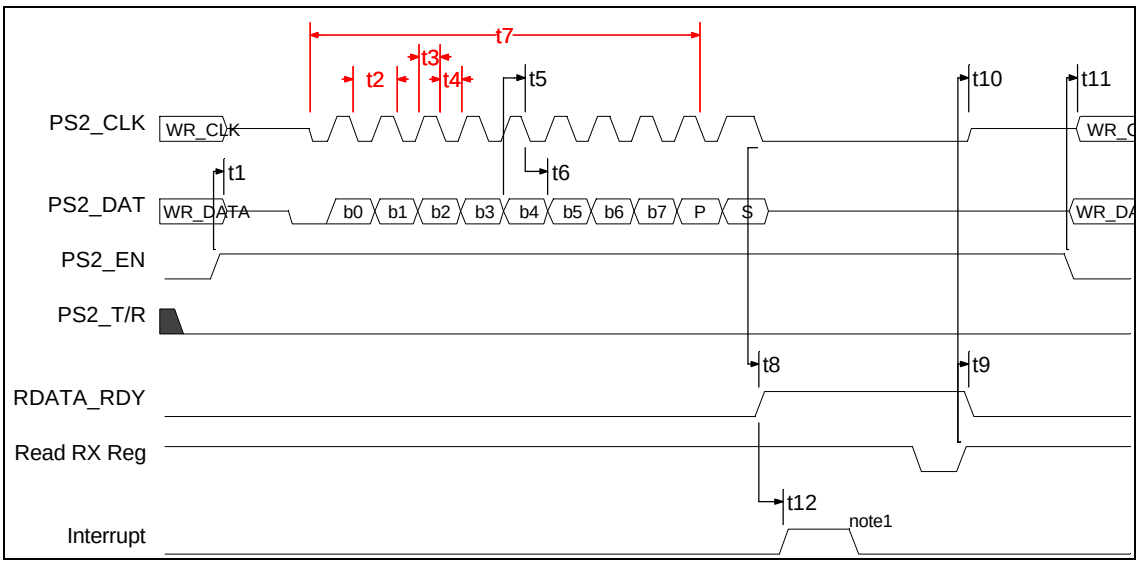


FIGURE 74 - PS/2 CHANNEL RECEIVE TIMING DIAGRAM

PS/2 CHANNEL RECEPTION PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	The PS2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			100	ns
t2	Period of CLK	60		302	us
t3	Duration of CLK high (active)	30		151	us
t4	Duration of CLK low (inactive)	30		151	us
t5	DATA setup time to falling edge of CLK. FDC37N972 samples the data line on the falling CLK edge.	1			us
t6	DATA hold time from falling edge of CLK. FDC37N972 samples the data line on the falling CLK edge.	2			us
t7	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t8	Falling edge of 11th CLK to RDATA_RDY asserted.			1.6	us

	PARAMETER	MIN	TYP	MAX	UNITS
t9	Trailing edge of the 8051's RD signal of the Receive Register to RDATA_RDY bit deasserted.			100	ns
t10	Trailing edge of the 8051's RD signal of the Receive Register to the CLK line released to high-Z.			100	ns
t11	The PS2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS2_EN is written to 0.			100	ns
t12	RDATA_RDY asserted to interrupt generated. Note1- Interrupt is cleared by reading the 8051 INT0 Source Register.			100	ns

PS/2 CHANNEL TRANSMIT TIMING DIAGRAM

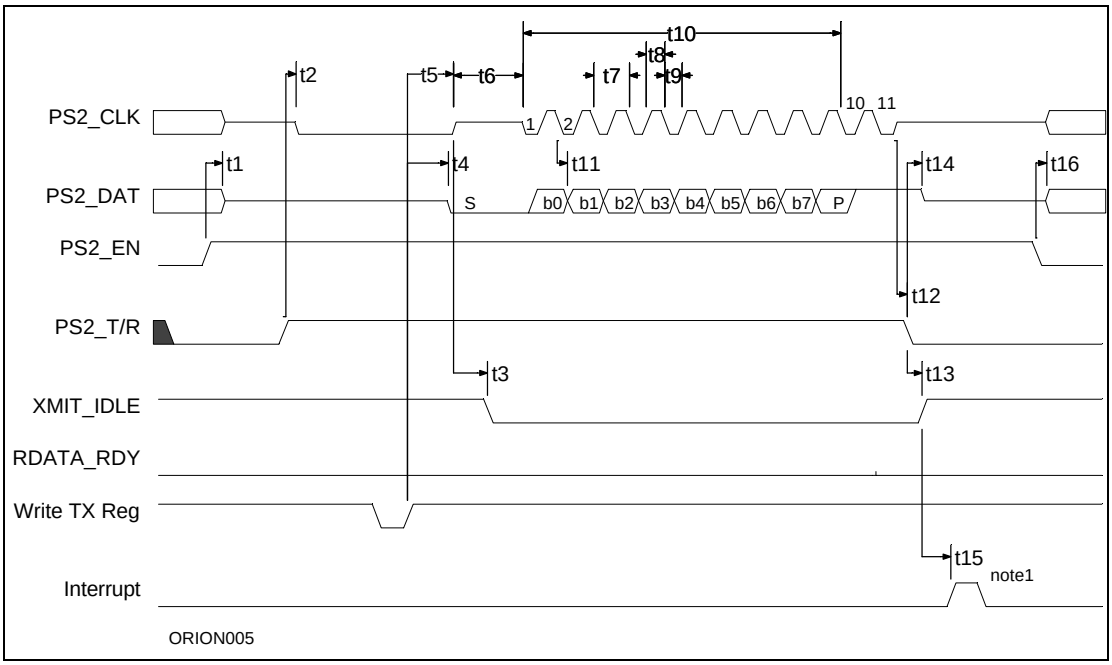


FIGURE 75 - PS/2 CHANNEL TRANSMIT TIMING DIAGRAM

PS/2 CHANNEL TRANSMISSION TIMING PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	The PS2 Channel's CLK and DATA lines are floated following PS2_EN=1 and PS2_T/R=0.			100	ns
t2	PS2_T/R bit set to CLK driven low preparing the PS2 Channel for data transmission.			100	ns
t3	CLK line floated to XMIT_IDLE bit deasserted.			1.7	us
t4	Trailing edge of 8051 WR of Transmit Register to DATA line driven low.	45		90	ns
t5	Trailing edge of 8051 WR of Transmit Register to CLK line floated.	90		130	ns

	PARAMETER	MIN	TYP	MAX	UNITS
t6	Initiation of Start of Transmit cycle by the PS2 channel controller to the auxilliary peripheral's responding by latching the Start bit and driving the CLK line low.	0.002		25.003	ms
t7	Period of CLK	60		302	us
t8	Duration of CLK high (active)	30		151	us
t9	Duration of CLK low (inactive)	30		151	us
t10	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t11	DATA output by FDC37N972 following the falling edge of CLK. The auxilliary peripheral device samples DATA following the rising edge of CLK.	3.5		7.1	us
t12	Rising edge following the 11th falling clock edge to PS_T/R bit driven low.	400		800	ns
t13	Trailing edge of PS_T/R to XMIT_IDLE bit asserted.			100	ns
t14	DATA released to high-Z following the PS2_T/R bit going low.			100	ns
t15	XMIT_IDLE bit driven high to interrupt generated. Note1- Interrupt is cleared by reading the 8051 INT0 Source Register.			100	ns
t16	The PS2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS2_EN is written to 0.			100	ns

PS/2 CHANNEL “BIT-BANG” TIMING

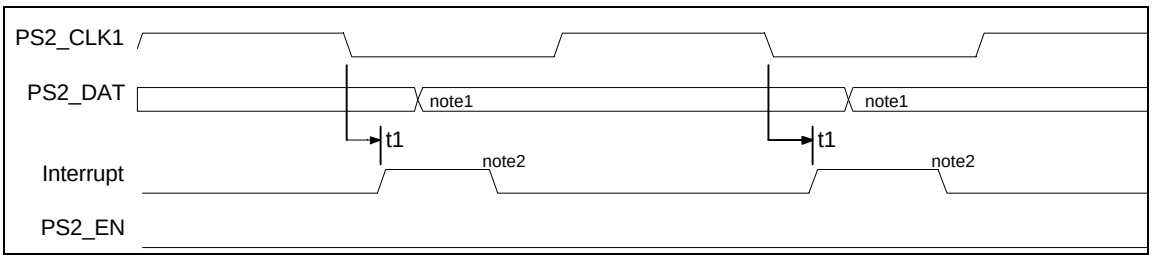


FIGURE 76 - PS/2 CHANNEL “BIT-BANG” TRANSMIT TIMING DIAGRAM

TABLE 250 - PS/2 CHANNEL “BIT-BANG” TRANSMIT TIMING PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	Falling Edge of CLK to Interrupt generated.			1.1	us
	8051 firmware responds to interrupt and drives data line before rising edge of PS2_CLK line.				
	8051 firmware clears Interrupt by reading the 8051 INT0 Source Register.				

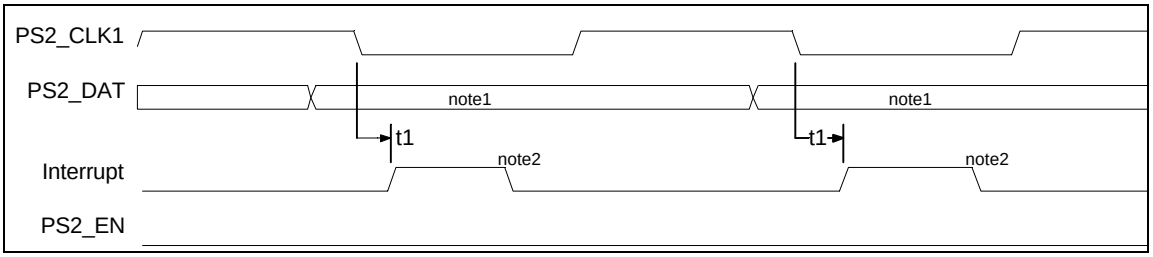


FIGURE 77 - PS/2 CHANNEL “BIT-BANG” RECEIVE TIMING DIAGRAM

TABLE 251 - PS/2 CHANNEL “BIT-BANG” RECEIVE TIMING PARAMETERS

	PARAMETER	MIN	TYP	MAX	UNITS
t1	Falling Edge of CLK to Interrupt generated.			100	ns
	8051 firmware responds to interrupt and latches data line before rising edge of PS2_CLK line.				
	8051 firmware clears Interrupt by reading the 8051 INT0 Source Register.				

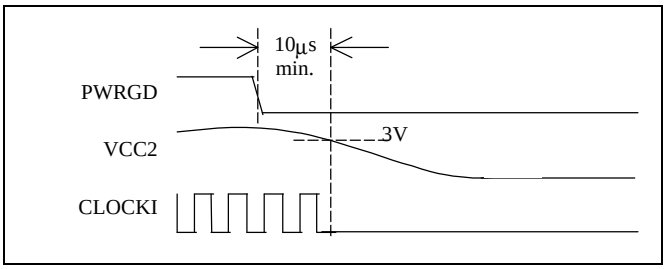


FIGURE 78 – POWER-FAIL EVENT

PARAMETER	MIN	TYP	MAX	UNITS
Valid CLOCKI to PWRGD Deasserted	10			µs

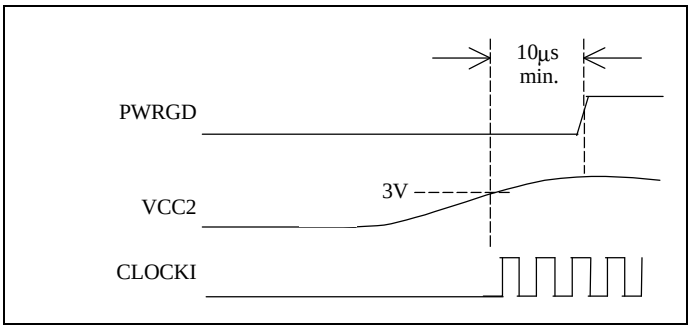


FIGURE 79 - VCC2 POWER-UP TIMING

PARAMETER	MIN	TYP	MAX	UNITS
Valid CLOCKI to PWRGD Asserted	10			µs

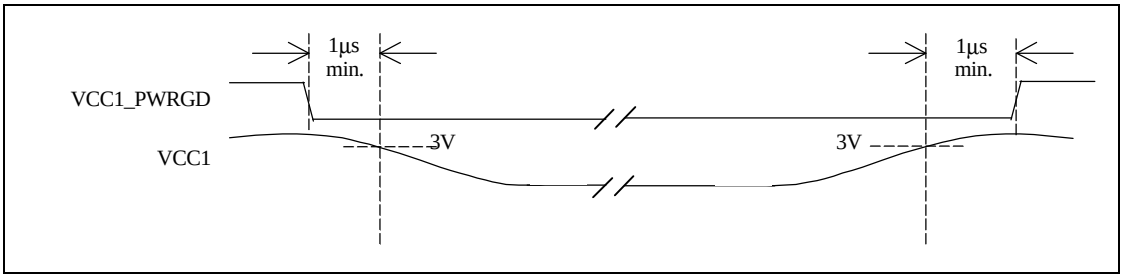


FIGURE 80 - VCC1_PWRGD TIMING

PARAMETER	MIN	TYP	MAX	UNITS
Valid VCC1 to VCC1_PWRGD Deasserted	1			µs
Valid VCC1 to VCC1_PWRGD Asserted	1			µs

IN CIRCUIT TEST (ICT)

The ICT impedance measurement is installed in the Production Test Program. It is run after Opens/Shorts (Vcc still at 0V). The measurement forces 0.2V on all ICT pins simultaneously and measures for less than 0.2uA. A failure at this time branches to a pin by pin test that forces 0.2V and measures 0.2uA on individual pins. Any pin greater then 0.2uA is considered a failure.

Table 252 - ICT PIN MAP

PIN #	PIN NAME
2	nDS1 / OUT5
3	nMTR1 / OUT6
9	nDIR
14	nINDEX
15	nTRK0
16	nWPRTPRT
17	nRDATA
18	nDSKCHG
19	FPD
20	IRTX
24	KSO11
25	KSO10
26	KSO9
27	KSO8
28	KSO7
30	KSO6
31	KSO5
32	KSO4
33	KSO3
34	KSO2
35	KSO1
36	KSO0
37	KS17
38	KS16
39	KS15
40	KS14
41	KS13
42	KS12
43	KS11
44	KS10
48	IMDAT
50	KCLK
51	KDAT
52	EMCLK
53	EMDAT
55	SA1

PIN #	PIN NAME
57	SA3
59	SA5
61	SA7
63	SA9
76	nNoWS
77	nIOR
78	nIOW
81	SD1
84	SD3
86	SD5
88	SD7
90	nDACK0
91	DRQ0
92	nDACK1
93	DRQ1
96	nROMCS
97	nMEMRD
98	nMEMWR
99	PCI_CLK
109	VCC1_PWRGD
110	nPWR_LED
141	RXD2 / GPIO8
151	IN3
154	IN6
157	XOSEL
190	GPIO6
193	nEA
194	MODE
195	AB_DATA
196	AB_CLK
197	nBAT_LED
203	OUT7
204	GPIO16
206	GPIO17
207	GPIO18
208	GPIO19

BOARD LEVEL CONNECTIVITY TEST MODE

To allow the FDC37N972 to be tested efficiently at board level, a test mode is provided to allow board level connectivity testing to be carried out. The board level connectivity test mode (AND tree mode) is defined below.

The AND tree test mode is enabled and latched by:

IOWb = IORb = MEMWRb = MEMRDb = 0 and PWRGD = 1

When activated, this test mode forces all output and bidirectional pins to function as inputs. All these input pins are now input to an AND tree which is output on nRESET_OUT. This will allow one single input pin, when switched, to toggle the nRESET_OUT output, if all other input pins are high.

This test mode is disabled/reset by a POR.

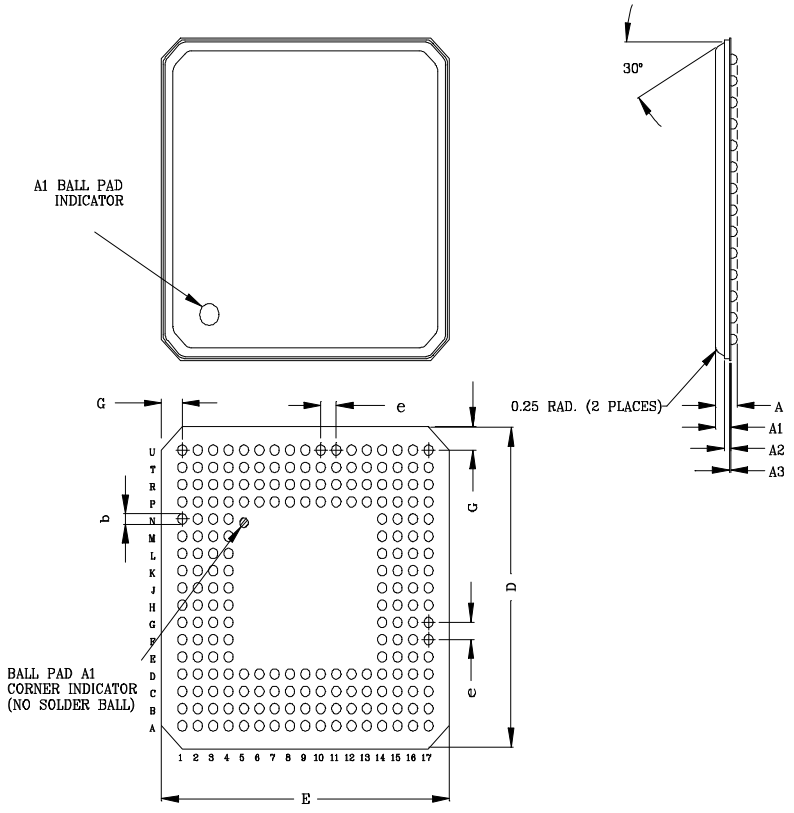
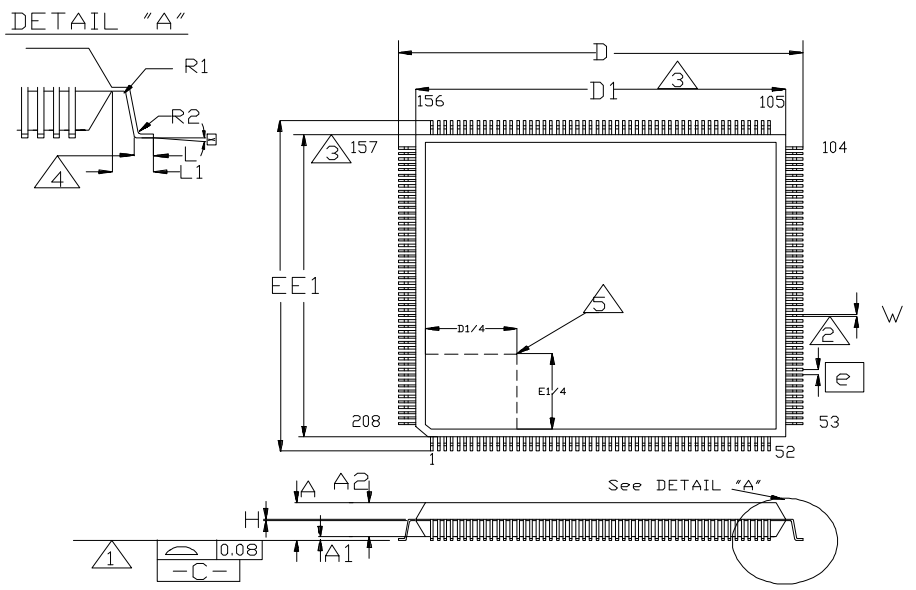


FIGURE 81 - 208 PIN FLEX BGA 15.0X15.0X1.10 (PRELIMINARY)



	MIN	NOM	MAX		MIN	NOM	MAX
A			1.6	L	0.45	0.60	0.75
A1	0.05		0.15	L1		1.00	
A2	1.35		1.45	e		0.50BSC	
D	29.90	30.00	30.10	θ	0°		7°
D1	27.90	28.00	28.10	W	0.17		0.27
E	29.90	30.00	30.10	R1	0.08		
E1	27.90	28.00	28.10	R2	0.08		0.20
H	0.09		0.230	ccc			0.08

Notes:

1) Coplanarity is 0.080 mm or 3.2 mils maximum
2) Tolerance on the position of the leads is 0.080 mm maximum
3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm
4) Dimensions for foot length L measured at the gauge plane 0.25 mm above the seating plane
5) Details of pin 1 identifier are optional but must be located within the zone indicated
6) Controlling dimension: millimeter

FIGURE 82 - 208 PIN TQFP PACKAGE OUTLINE

APPENDIX A

HIGH-PERFORMANCE 8051 CYCLE TIMING AND INSTRUCTION SET

The high-performance 8051 processor offers increased performance by executing instructions in a 4-clock cycle, as opposed to the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectutres.

Some instructions require a different number of instruction cycles on the high-performance 8051than they do on the standard 8051. In the standard 8051, all instructions except for MUL and DIV take one or two instruction cycles to complete. Int the high-performance 8051 architecture, instructions can take between one and five instructions to complete. The average speed improvement for the entire instruction set is approximately 2.5X.

LEGEND FOR INSTRUCTION SET TABLE

SYMBOL	FUNCTION
A	Accumulator
Rn	Register R7-R0
direct	Internal register address
@Ri	Internal register pointed to by R0 or R1 (except MOVX)
rel	Two's complement offset byte
bit	Direct bit address
#data	8-bit constant
#data 16	16-bit constant
addr 16	16-bit destination address
addr 11	11-bit destination address

TABLE 253 - 8051 INSTRUCTION SET

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
ARITHMETIC				
ADD A, Rn	Add register to A	1	1	28-2F
ADD A, direct	Add direct byte to A	2	2	25
ADD A, @Ri	Add data memory to A	1	1	26-27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	1	38-3F
ADDC A, direct	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add data memory to A with carry	1	1	36-37
ADDC A, #data	Add immediate to A with carry	2	2	34

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
SUBB A, Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A, direct	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract data memory from A with borrow	1	1	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	1	04
INC Rn	Increment register	1	1	08-0F
INC direct	Increment direct byte	2	2	05
INC @Ri	Increment data memory	1	1	06-07
DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC direct	Decrement direct byte	2	2	15
DEC @Ri	Decrement data memory	1	1	16-17
INC DPTR	Increment data pointer	1	3	A3
MUL AB	Multiply A by B	1	5	A4
DIV AB	Divide A by B	1	5	84
DA A	Decimal adjust A	1	1	D4
LOGICAL				
ANL A, Rn	AND register to A	1	1	58-5F
ANL A, direct	AND direct byte to A	2	2	55
ANL A, @Ri	AND data memory to A	1	1	56-57
ANL A, #data	AND immediate to A	2	2	54
ANL direct, A	AND A to direct byte	2	2	52
ANL direct, #data	AND immediate data to direct byte	3	3	53
ORL A, Rn	OR register to A	1	1	48-4F
ORL A, direct	OR direct byte to A	2	2	45
ORL A, @Ri	OR data memory to A	1	1	46-47
ORL A, #data	OR immediate to A	2	2	44
ORL direct, A	OR A to direct byte	2	2	42
ORL direct, #data	OR immediate data to direct byte	3	3	43
XORL A, Rn	Exclusive-OR register to A	1	1	68-6F
XORL A, direct	Exclusive-OR direct byte to A	2	2	65
XORL A, @Ri	Exclusive-OR data memory to A	1	1	66-67

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
XORL A, #data	Exclusive-OR immediate to A	2	2	64
XORL direct, A	Exclusive-OR A to direct byte	3	3	63
XORL direct, #data	Exclusive-OR immediate to direct byte	3	3	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13
DATA TRANSFER				
MOV A, RN	Move register to A	1	1	E8-EF
MOV A, direct	Move direct byte to A	2	2	E5
MOV A, @Ri	Move data memory to A	1	1	E6-E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to reigster	1	1	F8-FF
MOV Rn, direct	Move direct byte to register	2	2	A8-AF
MOV Rn, #data	Move immediate to register	2	2	78-7F
MOV direct, A	Move A to direct byte	2	2	F5
MOV direct, Rn	Move register to direct byte	2	2	88-8F
MOV direct, direct	Move direct byte to direct byte	3	3	85
MOV direct, @Ri	Move data memory to direct byte	2	2	86-87
MOV direct, #data	Move immediate to direct byte	3	3	75
MOV @Ri, A	Move A to data memory	1	1	F6-F7
MOV @Ri, direct	Move direct byte to data memory	2	2	A6-A7
MOV @Ri, #data	Move immediate to data memory	2	2	76-77
MOV DPTR, #data	Move immediate to data pointer	3	3	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	3	93

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
MOVC A, @A+PC	Move code byte relative PC to A	1	3	83
MOVX A, @Ri	Move external data (A8) to A	1	2-9	E2-E3
MOVX A, @DPTR	Move external data (A16) to A	1	2-9	E0
MOVX @Ri, A	Move A to external data (A8)	1	2-9	F2-F3
MOVX @DPTR, A	Move A to external data (A16)	1	2-9	F0
PUSH direct	Push direct byte onto stack	2	2	C0
POP direct	Pop direct byte from stack	2	2	D0
XCH A, Rn	Exchange A and register	1	1	C8-CF
XCH A, direct	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and data memory	1	1	C6-C7
XCHD A, @Ri	Exchange A and data memory nibble	1	1	D6-D7
Boolean				
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set Carry	1	1	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	2	82
ANL C, /bit	AND direct bit inverse to carry	2	2	B0
ORL C, bit	OR direct bit to carry	2	2	72
ORL C, /bit	OR direct bit inverse to carry	2	2	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	2	92
BRANCHING				
ACALL addr 11	Absolute call to subroutine	2	3	11-F1
LCALL addr 16	Long call to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32

INSTRUCTION	DESCRIPTION	BYTE COUNT	INSTRUCTION CYCLES	HEX CODE
AJMP addr 11	Absolute jump unconditional	2	3	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	3	80
JC rel	Jump on carry = 1	2	3	40
JNC rel	Jump on carry = 0	2	3	50
JB bit, rel	Jump on direct bit = 1	3	4	20
JNB bit, rel	Jump on direct bit = 0	3	4	30
JMP @A+DPTR	Jump indirect relative DPTR	1	3	73
JZ rel	Jump on accumulator = 0	2	3	60
JNZ rel	Jump on accumulator /= 0	2	3	70
CJNE A, direct, rel	Compare A, direct JNE relative	3	4	B5
CJNE A, #d, rel	Compare A, immediate JNE relative	3	4	B4
CJNE Rn, #d, rel	Compare reg, immediate JNE relative	3	4	B8-BF
CJNE @Ri, #d, rel	Compare Ind, immediate JNE relative	3	4	B6-B7
DJNZ Rn, rel	Decrement register, JNZ relative	2	3	D8-DF
DJNZ direct, rel	Decrement direct byte, JNZ relative	3	4	D5
MISCELLANEOUS				
NOP	No operation	1	1	00

APPENDIX B

HIGH PERFORMANCE 8051 EXTENDED INTERRUPT UNIT

Interrupts

The EXIF, EICON, EIE, and EIP registers provide flags, enable control, and priority control for the extended interrupt unit in the FDC37N972 high-performance 8051.

Interrupt Processing

When an enabled interrupt occurs, the CPU vectors to the address of the interrupt service routine (ISR) associated with that interrupt (See TABLE 92 - 8051 INTERRUPTS on page 169). The CPU executes the ISR to completion unless another interrupt of higher priority occurs. Each ISR ends with a RETI (return from interrupt) instruction. After executing the RETI, the CPU returns to the next instruction that would have been executed if the interrupt had not occurred.

An ISR can only be interrupted by a higher priority interrupt. That is, an ISR for a low-level interrupt can only be interrupted by high-level interrupt. An ISR for a high-level interrupt can only be interrupted by the power-fail interrupt (extended interrupt unit only).

The 8051 always completes the instruction in progress before servicing an interrupt. If the instruction in progress is RETI, or a write access to any of the IP, IE, EIP, or EIE SFRs, the 8051 completes one additional instruction before servicing the interrupt.

Interrupt Masking

The EA bit in the IE SFR (IE.7) is a global enable for all interrupts except the power-fail interrupt. When EA = 1, each interrupt is enabled/masked by its individual enable bit. When EA = 0, all interrupts are masked. The only exception is the power-fail interrupt, which is not affected by the EA bit. When EPFI = 1, the power-fail interrupt is enabled, regardless of the state of the EA bit. TABLE 92 on page 169 provides a summary of interrupt sources, flags, enables, and priorities.

Interrupt Priorities

There are two stages of interrupt priority assignment, interrupt level and natural priority. The interrupt level (highest, high, or low) takes precedence over natural priority. The power-fail interrupt, if enabled, always has highest priority and is the only interrupt that can have highest priority. All other interrupts can be assigned either high or low priority.

In addition to an assigned priority level (high or low), each interrupt also has a natural priority, as listed in TABLE 92 - on page 169. Simultaneous interrupts with the same priority level (for example, both high) are resolved according to their natural priority. For example, if int0_n and int2 are both programmed as high priority, int0_n takes precedence.

Once an interrupt is being serviced, only an interrupt of higher priority level can interrupt the service routine of the interrupt currently being serviced.

Interrupt Sampling

The internal timers and serial ports generate interrupts by setting their respective SFR interrupt flag bits. External interrupts are sampled once per instruction cycle.

int0_n and int1_n are both active low and can be programmed to be either edge-sensitive or level-sensitive, through the IT0 and IT1 bits in the TCON SFR. For example, when IT0 = 0, int0_n is level-sensitive and the 8051 sets the IE0 flag when the int0_n pin is sampled low. When IT0 = 1, int0_n is edge-sensitive and 8051 sets the IE0 flag when the int0_n pin is sampled high then low on consecutive samples.

The remaining four external interrupts are edge-sensitive only. int2 and int4 are active high, int3_n and int5_n are active low. The power-fail (pfi) interrupt is edge-sensitive, active high, and sampled once per instruction cycle. To ensure that edge-sensitive interrupts are detected, the corresponding ports should be held high for 4 clk cycles and then low for 4 clk cycles. Level-sensitive interrupts are not latched and must remain active until serviced.

Interrupt Latency

Interrupt response time depends on the current state of the 8051. The fastest response time is 5 instruction cycles: 1 to detect the interrupt, and 4 to perform the LCALL to the ISR. The maximum latency (13 instruction cycles) occurs when the 8051 is currently executing a RETI instruction followed by a MUL or DIV instruction. The 13 instruction cycles in this case are: 1 to detect the interrupt, 3 to complete the RETI, 5 to execute the DIV or MUL, and 4 to execute the LCALL to the ISR. For the maximum latency case, the response time is 13 x 4 = 52 clk cycles.

Dual Data Pointers

The high-performance 8051 in the FDC37N972 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external RAM or peripherals. The FDC37N972 maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h. It is not necessary to modify code to use DPTR0.

The FDC37N972 adds a second data pointer (DPTR1) at SFR locations 84h and 85h. The SEL bit in the DPTR Select Register, DPS (SFR 86h), selects the active pointer (see sections **DPL1**, DPH1 and DPS below).

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move.

Timer 2

Overview

The high-performance 8051 in the FDC37N972 includes a third timer/counter (Timer 2). Timer 2 runs only in 16-bit mode and offers several capabilities not available with Timers 0 and 1. The modes available with Timer 2 are 16-bit auto-reload timer/counter and baud rate generator. The SFRs associated with Timer 2 are:

- T2CON (SFR C8h)
- RCAP2L (SFR CAh) – Used as the 16-bit LSB reload value when Timer 2 is configured for auto-reload mode.
- RCAP2H (SFR CBh) – Used as the 16-bit MSB reload value when Timer 2 is configured for auto-reload mode.
- TL2 (SFR CCh) – Lower 8 bits of 16-bit count.
- TH2 (SFR CDh) – Upper 8 bits of 16-bit count.

TABLE 254 summarizes how the T2CON SFR bits (TABLE 259) determine the Timer 2 operating mode.

TABLE 254 - TIMER 2 MODE CONTROL SUMMARY

RCLK	TCLK	TR2	MODE
0	0	1	16-bit Timer/Counter w/Auto-reload
1	X	1	Baud Rate Generator
X	1	1	Baud Rate Generator
X	X	0	Off

16-bit Timer/Counter Mode with Auto-reload

FIGURE 83 illustrates how Timer 2 operates in timer/counter mode with auto-reload. The 16-bit timer counts CLK cycles (divided by 4 or 12). The TR2 bit enables the counter. When the count increments from FFFFh, the overflow occurs. The overflow causes the TF2 flag is set, and t2_out goes high for one CLK cycle. The overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

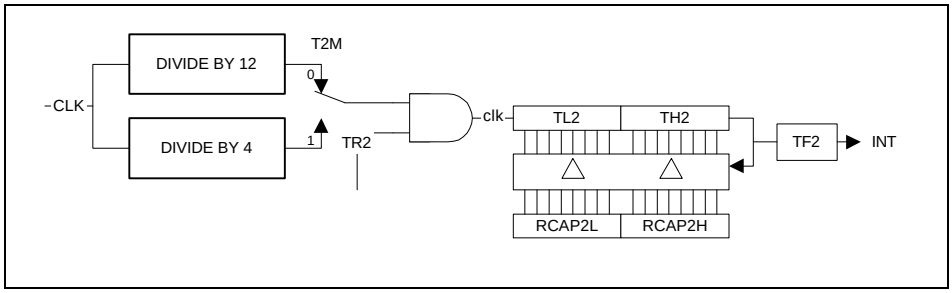


FIGURE 83 - TIMER 2 TIMER/COUNTER WITH AUTO-RELOAD

Baud Rate Generator Mode

Setting either RCLK or TCLK to 1 configures Timer 2 to generate baud rates for Serial Port 0 in serial mode 1 or 3. In baud rate generator mode, Timer 2 functions in auto-reload mode. However, instead of setting the TF2 flag, the counter overflow is used to generate a shift clock for the serial port function. As in normal auto-reload mode, the overflow also causes the preloaded start value in the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers.

When either TCLK = 1 or RCLK = 1, Timer 2 is forced into auto-reload operation. The counter time base in baud rate generator mode is clk/2.

Special Function Registers

The following SFRs are not part of the sandard 8051 architecture.

DPL1

The DPL1 register (TABLE 255) is the LSB of DPTR1 (see the section interrupts above).

TABLE 255 - DPL1 REGISTER - SFR 84H

SFR ADDRESS	84h
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	A7	A6	A5	A4	A3	A2	A1	A0

DPH1

The DPH1 register (**TABLE 256**) is the MSB of DPTR1 (see the section interrupts above).

TABLE 256 - DPH1 REGISTER - SFR 85H

SFR ADDRESS	85h
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	A15	A14	A13	A12	A11	A10	A9	A8

DPS

The DPS register (**TABLE 257**) is used to select the active DPTR (see the section interrupts above).

TABLE 257 - DPS REGISTER - SFR 86H

SFR ADDRESS	86h
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R**	**R**	**R**	**R**	**R**	**R**	**R**	**R/W**
BIT NAME	RESERVED							SEL[1]

NOTE[1] When SEL = ‘0’, instructions that use the DPTR will use DPL0 and DPH0. When SEL = ‘1’, instructions that use the DPTR will use DPL1 and DPH1.

CKCON

The default timer clock scheme for the DW8051 timers is 12 clk cycles per increment, the same as in the standard 8051. However, in the DW8051, the instruction cycle is 4 clk cycles. Using the default rate (12 clocks per timer increment) allows existing application code with real-time dependencies, such as baud rate, to operate properly. However, applications that require fast timing can set the timers to increment every 4 clk cycles by setting bits in the Clock Control register (CKCON) at SFR location 8Eh (**TABLE 258** and **TABLE 259**).

The CKCON bits that control the timer clock rates are:

CKCON BIT	COUNTER/TIMER
5	Timer 2
4	Timer 1
3	Timer 0

When a CKCON register bit is set to 1, the associated counter increments at 4-clk intervals. When a CKCON bit is cleared, the associated counter increments at 12-clk intervals. The timer controls are independent of each other. The default setting for all three timers is 0 (12-clk intervals). These bits have no effect in counter mode.

TABLE 258 - CKCON REGISTER - SFR 8EH

SFR ADDRESS	8EH
POWER	VCC1
DEFAULT	0x01

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RESERVED		T2M	T1M	T0M	MD2	MD1	MD0

TABLE 259 - CKCON REGISTER BIT DESCRIPTIONS

BIT	FUNCTION
CKCON.7-6	Reserved
CKCON.5	T2M. Timer 2 clock select. When T2M = 0, Timer 2 uses clk/12 (for compatibility with 80C32); when T2M = 1, Timer 2 uses clk/4. This bit has no effect when Timer 2 is configured for baud rate generation.
CKCON.4	T1M. Timer 1 clock select. When T1M = 0, Timer 1 uses clk/12 (for compatibility with 80C32); when T1M = 1, Timer 1 uses clk/4.
CKCON.3	T0M. Timer 0 clock select. When T0M = 0, Timer 0 uses clk/12 (for compatibility with 80C32); when T0M = 1, Timer 0 uses clk/4.
CKCON.2-0	MD2, MD1, MD0 -- Control the number of cycles to be used for external MOVX instructions.

MPAGE

The MPAGE special function register (**TABLE 260**) replaces the function of the Port 2 latch in the FDC37N972. During MOVX A, @Ri and MOVX @Ri, A instructions, the 8051 places the contents of the MPAGE register on the upper eight address bits. This provides the paging function that is normally provided by the Port 2 latch.

TABLE 260 - MPAGE REGISTER – SFR 92H

SFR ADDRESS	92H
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	A15	A14	A13	A12	A11	A10	A9	A8

T2CON

The T2CON register (TABLE 261 and TABLE 263) is used to configure Timer 2 (see the section **Interrupts** above).

TABLE 261 – T2CON REGISTER - SFR C8H

SFR ADDRESS	C8h
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	TF2	RESERVED	RCLK	TCLK	RESERVED	TR2	RESERVED	

TABLE 263 – T2CON REGISTER BIT DESCRIPTIONS

BIT	FUNCTION
T2CON.7	TF2 Timer 2 overflow flag. Hardware will set TF2 when the Timer 2 overflows from FFFFh. TF2 must be cleared to 0 by the software. TF2 will only be set to a 1 if RCLK and TCLK are both cleared to 0. Writing a 1 to TF2 forces a Timer 2 interrupt if enabled.
T2CON.6	Reserved. This bit should be written as '0'.
T2CON.5	RCLK Receive clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of received data in serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the receive clock. RCLK =0 selects Timer 1 overflow as the receive clock.
T2CON.4	TCLK Transmit clock flag. Determines whether Timer 1 or Timer 2 is used for Serial Port 0 timing of transmit data in

BIT	FUNCTION
	serial mode 1 or 3. RCLK =1 selects Timer 2 overflow as the transmit clock. RCLK =0 selects Timer 1 overflow as the transmit clock.
T2CON.3	Reserved. This bit should be written as '0'.
T2CON.2	TR2. Timer 2 run control flag. TR2 = 1 starts Timer 2. TR2 = 0 stops Timer 2.
T2CON.1-0	Reserved. This bit should be written as '0'.

RCAP2L

The RCAP2L register (TABLE 263) is the 16-bit LSB reload value (RV[7:0]) when Timer 2 is configured for auto-reload mode (see the section interrupts above).

TABLE 263 - RCAP2L REGISTER – SFR CAH

SFR ADDRESS	CAh
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0

RCAP2H

The RCAP2H register (TABLE 264) is the 16-bit MSB reload value (RV[15:8]) when Timer 2 is configured for auto-reload mode (see the section interrupts above).

TABLE 264 - RCAP2H REGISTER - SFR CBH

SFR ADDRESS	CBh
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RV15	RV14	RV13	RV12	RV11	RV10	RV9	RV8

TL2

The TL2 register (TABLE 265) is the 16-bit LSB Timer 2 count value (CV[7:0]) (see the section **Interrupts** above).

TABLE 265 - TL2 REGISTER - SFR CCH

SFR ADDRESS	CCh
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0

TH2

The TH2 register (Table 266

TABLE 266) is the 16-bit MSB Timer 2 count value (CV[15:8]) (see the section interrupts above).

TABLE 266 - TH2 REGISTER - SFR CDH

SFR ADDRESS	CDh
POWER	VCC1
DEFAULT	0x00

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	CV15	CV14	CV13	CV12	CV11	CV10	CV9	CV8

EXIF

The EXIF register (Table 268 and Table 269) contains the external interrupt flags for the extended interrupt unit (see the section interrupts above).

TABLE 267 - EXIF REGISTER - SFR 91H

SFR ADDRESS	91h
POWER	VCC1
DEFAULT	0x08

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R**	**R**	**R**	**R**
BIT NAME	IE5	IE4	IE3	IE2	RESERVED			

TABLE 268 - EXIF REGISTER BIT DESCRIPTIONS

BIT	FUNCTION
EXIF.7	IE5 External Interrupt 5 flag. IE5 = 1 indicates a falling edge was detected at the int5_n pin. IE5 must be cleared by software. Setting IE5 in software generates an interrupt, if enabled.
EXIF.6	IE4 External Interrupt 4 flag. IE4 = 1 indicates a rising edge was detected at the int4 pin. IE4 must be cleared by software. Setting IE4 in software generates an interrupt, if enabled.
EXIF.5	IE3 External Interrupt 3 flag. IE3 = 1 indicates a falling edge was detected at the int3_n pin. IE3 must be cleared by software. Setting IE3 in software generates an interrupt, if enabled.
EXIF.4	IE2 External Interrupt 2 flag. IE2 = 1 indicates a rising edge was detected at the int2 pin. IE2 must be cleared by software. Setting IE2 in software generates an interrupt, if enabled.
EXIF.3	Reserved. Read as '1'.
EXIF.2-0	Reserved. Read as '0'.

EICON

The EICON register (TABLE 269 and TABLE 270) contains pfi and serial port 1 controls for the extended interrupt unit (see the section interrupts above).

TABLE 269 - EICON REGISTER - SFR D8H

SFR ADDRESS	D8h
POWER	VCC1
DEFAULT	0x40

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R/W**	**R/W**	**R/W**	**R/W**	**R**	**R**	**R**	**R**
BIT NAME	SMOD1	RESERVED	EPFI	PFI	RESERVED			

TABLE 270 - EICON REGISTER BIT DESCRIPTIONS

BIT	FUNCTION
EICON.7	SMOD1 Serial Port 1 baud rate doubler enable. When SMOD1 = 1, the baud rate for Serial Port 1 is doubled.
EICON.6	Reserved. Read as '1'.
EICON.5	EPFI Enable power-fail interrupt. EPFI = 0 disables power-fail interrupt (pfi). EPFI = 1 enables interrupts generated by the pfi pin.
EICON.4	PFI Power-fail interrupt flag. PFI = 1 indicates a power-fail

BIT	FUNCTION
	interrupt was detected at the pfi pin. PFI must be cleared by software before exiting the interrupt service routine. Otherwise, the interrupt occurs again. Setting PFI in software generates a power-fail interrupt, if enabled.
EICON.3-0	Reserved. Read as '0'.

EIE

The EIE register (Table 273 and Table 275) contains the external interrupt enables for the extended interrupt unit (see the section interrupts above).

TABLE 271 - EIE REGISTER - SFR E8H

SFR ADDRESS	E8h
POWER	VCC1
DEFAULT	0xE0

	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	**R**	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RESERVED				EX5	EX4	EX3	EX2

TABLE 272 - EIE REGISTER BIT DESCRIPTIONS

BIT	FUNCTION
EIE.7-5	Reserved. Read as '1'.
EIE.4	Reserved. Read and Write as '0'.
EIE.3	EX5 Enable external interrupt 5. EX5 = 0 disables external interrupt 5 (int5_n). EX5 = 1 enables interrupts generated by the int5_n pin.
EIE.2	EX4 Enable external interrupt 4. EX4 = 0 disables external interrupt 4 (int4). EX4 = 1 enables interrupts generated by the int4 pin.
EIE.1	EX3 Enable external interrupt 3. EX3 = 0 disables external interrupt 3 (int3_n). EX3 = 1 enables interrupts generated by the int3_n pin.
EIE.0	EX2 Enable external interrupt 2. EX2 = 0 disables external interrupt 2 (int2). EX2 = 1 enables interrupts generated by the int2 pin.

EIP

The EIP register (Table 273 and Table 274) contains the external interrupt priority controls for the extended interrupt unit (see the section interrupts above).

TABLE 273 - EIP REGISTER - SFR F8H

SFR ADDRESS	F8h
POWER	VCC1
DEFAULT	0xE0

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
TYPE	**R**	**R**	**R**	**R**	**R/W**	**R/W**	**R/W**	**R/W**
BIT NAME	RESERVED				PX5	PX4	PX3	PX2

TABLE 274 - EIP REGSITER BIT DESCRIPTIONS

BIT	**FUNCTION**
EIP.7-5	Reserved. Read as '1'.
EIP.4	Reserved. Read and Write as '0'.
EIP.3	PX5 External interrupt 5 priority control. PX5 = 0 sets external interrupt 5 (int5_n) to low priority. PX5 = 1 sets external interrupt 5 to high priority.
EIP.2	PX4 External interrupt 4 priority control. PX4 = 0 sets external interrupt 4 (int4) to low priority. PX2 = 1 sets external interrupt 4 to high priority.
EIP.1	PX3 External interrupt 3 priority control. PX3 = 0 sets external interrupt 3 (int3_n) to low priority. PX3 = 1 sets external interrupt 3 to high priority.
EIP.0	PX2 External interrupt 2 priority control. PX2 = 0 sets external interrupt 2 (int2) to low priority. PX2 = 1 sets external interrupt 2 to high priority.

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